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AK3671(B) Mobile Multimedia Application Processor

Specification

(applicable to AK3671 and AK3671B)

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Document Revision History

The following table provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

VERSION	DESCRIPTION	DATE COMPLETED
0.1.0	**Initial release**	October, 2009
0.2.0	**1) Section 3.20.1.4 & Section 3.20.3:** Modified Figure 3-41 Microphone Interface Architecture and Figure 3-44 Line in Interface. **2) Section 5.2.2:** Added the package information of AK3671B.	October, 2009

About This Manual

This document is the electrical and mechanical specification data sheet for the AK3671 and AK3671B processors. This specification contains a functional overview, mechanical data, package signal locations, electrical specifications (simulated), and bus functional waveforms.

Definitions, Acronyms, and Abbreviations

Unless otherwise specified, all the acronyms and abbreviations used in this manual are defined hereunder.

ADC	Analog to Digital Converter
AHB	Advanced High-performance Bus
ASIC	Application-Specific Integrated Circuit, refers to all the functional blocks of the processor
CMOS	Complimentary Metal-Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMA	Direct Memory Access
ECC	Error Correction Code
FIFO	First In First Out
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
JPEG	Joint Picture Expert Group
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MMC	Multimedia Card
MMU	Memory Management Unit
MPEG	Moving Picture Experts Group
MSB	Most Significant Bit
PMU	Power Management Unit
PGA	Programmable Gain Amplifier
PWM	Pulse-Width Modulator
PLL	Phase Locked Loop
QFP	Qual Flat Package
RAM	Random Access Memory
ROM	Read Only Memory

RTC	Real Time Clock
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XTAL	Crystal

1 Introduction

As new members of AK36XX series mobile multimedia application processors, AK3671(B) application processors are designed specially to bring industry-leading multimedia performance and high system integration for digital products. Compared with their compeers, AK3671(B) integrates more functional blocks, such as LDOs, camera interface, video encoders, etc., and enhances the performance, such as PMU efficiency.

AK3671(B) features the advanced and power-efficient 32-bit microprocessor core. Integrated with a powerful video decoder, a high-performance audio decoder, an image processor, a 10-bit SAR ADC, a 16-bit sigma-delta ADC, two 18-bit Sigma-Delta DACs, a power amplifier, a headphone driver, a USB 2.0 HS Device controller, a Multimedia Card/Secure Digital Host Controller (MMC/SD), and Power Management Unit (PMU), AK3671(B) offers a suite of peripherals to enable any product to provide rich multimedia experience at low cost and in small dimension. In addition, the AK3671(B) application processors are packaged in QFP, which is convenient and handy for the manufacturing and maintenance of final devices.

For cost-sensitive applications, the Nand Flash controller allows low-cost Nand Flash devices to be used as main non-volatile storage, on which the boot code can be saved. And the on-chip ECC circuitry of Nand Flash controller improves the reliability of data and code.

Unless otherwise specified, this specification is applicable to AK3671 and AK3671B. It should be noted that AK3671 and AK3671B are the same with the exception of their packages: AK3671 (QFP package) and AK3671B (BGA package). In the following sections only the AK3671 is described.

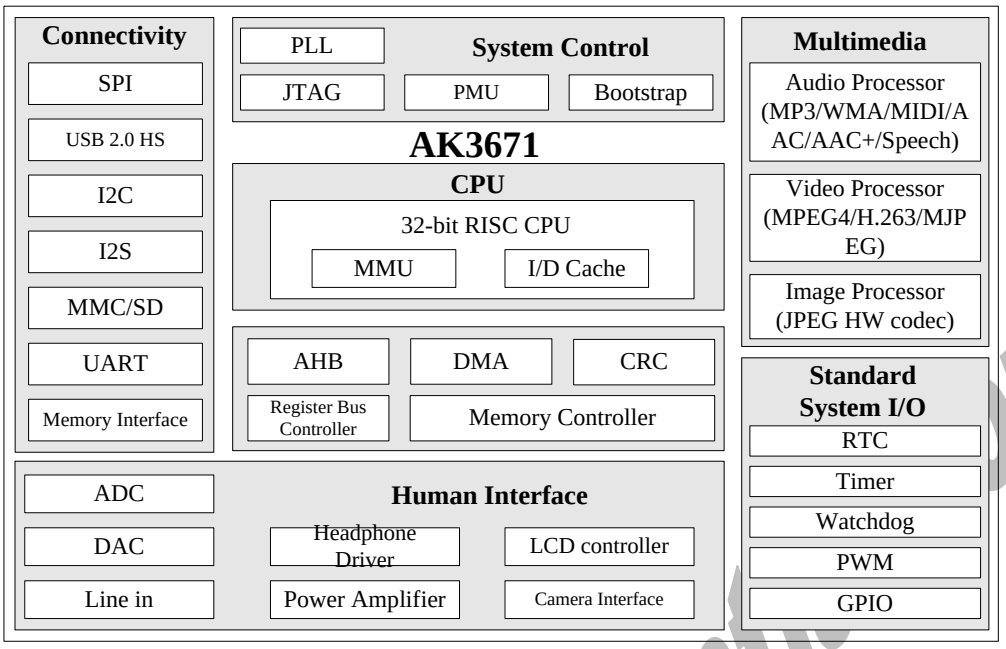


Figure 1-1. AK3671 Functional Block Diagram

1.1 Conventions

- #*Abc* is used to indicate a signal that is active when pulled low: for example, #Reset.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
- *Negated* means that an asserted discrete signal changes logic state.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers ended in letter *B* are binary. Numbers preceded by *0x* are hexadecimal.

1.2 Features

To support a wide variety of applications, AK3671 boasts a robust array of features, including the following:

- 32-bit microprocessor core, integrated I/D cache with MMU capability
- up to 184MHz CPU clock and 92MHz system operating frequency
- advanced power management module
- high-efficient PMU, including one DC-DC regulator and one LDO
- supports little endian only
- supports 64MB SDRAM
- supports up to two pieces of NAND FLASH with ECC function (hardware generation, detection, indication and software correction)
- embedded audio processor with real-time AMR codec/ MP3 decoder/ WMA decoder/ 64-tone MIDI synthesizer/AAC decoder/AAC+ decoder, supporting audio stream in PCM/ADPCM format
- H.263 decoder and encoder, CIF30fps@60MHz
- MJPEG decoder and encoder, CIF30fps@60MHz
- MPEG4-SP. level 1, 2&3 decoder and encoder, CIF30fps@60MHz
- JPEG decoder and encoder
- software I2C
- CCIR 601/CCIR 656 CMOS image sensor interface with programmable image size and smart scaling capability
- 16-bit/9-bit/8-bit MPU display with programmable LCD size
- one 16-bit sigma-delta ADC for voice recording
- one 10-bit ADC including four channels for touch screen, one channel for battery measurement, and one general-purpose input channel
- two 18-bit Sigma-Delta DACs for stereo speakers
- Class AB power amplifier (620mW maximum output at SPVDD =3.6V)
- built-in headphone driver
- built-in vibrator and LED control in synchronization with music
- master/slave I2S interface
- one UART
- one SPI (master or slave operation)
- MMC/SD interface, MMC 4.0; SD 2.0

- USB 2.0 HS Device
- Thirty-one GPIOs, three dedicated, twenty-eight as GPIOs and shared with other pins
- JTAG supporting in-circuit debugging
- on-chip PLL and 32.768KHz RTC
- one PWM
- three General Purpose timers
- one watchdog timer
- one RTC watchdog timer
- four bootstrap modes
- package:

  AK3671: 144-pin QFP

  AK3671B: 144-pin BGA

1.3 Target Applications

The AK3671 targets Portable Media Players (PMPs), Electronic Learning Machines (ELMs), digital audio/video players, portable handheld devices, and other advanced multimedia appliances.

1.4 Product Documentation

The following document(s) is (are) required for a complete description of the AK3671(B) and are necessary to design properly with the device.

- *AK3671(B) Programmer's Guide*

1.5 Ordering Information

PART NUMBER	PACKAGE TYPE	OPERATING VOLTAGE	ORDER NUMBER
AK3671Q144	144-pin QFP	I/O: 2.97V~3.63V, core: 1.62~1.98V	
AK3671B144	144-pin BGA	I/O: 2.97V~3.63V, core: 1.62~1.98V	

2 Signals and Connections

2.1 Pin Definitions

Table 2-1 identifies and describes the AK3671 signals that are assigned to package pins. The pin definitions are grouped by the internal modules they are connected to.

Table 2-1 AK3671 Functional Pin Definitions

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
1. Reset and Clock (8)					
#RST	I	D	PU	I	System reset, external active low Schmitt trigger input signal. When this signal is active, all modules (with the exception of RTC module) are reset.
watch_dog	O	D	PPU	I/PU	Watchdog timer (Timer 4) has reached 0 state indicator, low active.
XTAL12MI	I	D	-	-	External 12MHz crystal input.
XTAL12MO	O	D	-	-	External 12MHz crystal output.
PCLK_OUT	O	D	PPU	O	A programmable clock output, controlled by Clock Divider Register.
XTAL32KI	I	D	-	-	External 32.768KHz crystal input.
XTAL32KO	O	D	-	-	External 32.768KHz crystal output.
RTC_WU_WD	O	D	-	O/Z	RTC wakeup/watch dog indicator for power control processing (active high pulse indicator to Power Supply.)
2. USB2.0 Interface (4)					
DP	I/O	A	-	-	USB Data pin, Data+.
DM	I/O	A	-	-	USB Data pin, Data-.
VDDA	I/O	A	-	-	This pin should tie a 0.1u capacitor to VSS(USB).
RREF	I/O	A	-	-	External reference pin. It is recommended to connect a 10K ohm external reference resistor, with 1% tolerance to analog ground.
3. Audio/Analog Interface (18)					

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
R100K_TS	I/O	A	-	-	Reference PIN, connecting an external 100K-ohm resistor between this pin and ground. The resistor employed here is to provide a bias current for the Opamp(ADC's internal amplifier).
VCM	I	A	-	-	ADC2 mid rail voltage decoupling input. It is recommended to parallel connect a 10uF capacitor and a 0.1uF capacitor between this pin and ground. Voltage level is 1/2 AVDD.
HPL	O	A	-	-	Audio headphone left output.
HPR	O	A	-	-	Audio headphone right output.
Line_in	I	A	-	-	Mono line in.
SPKPLUS	O	A	-	-	Audio speaker differential output plus.
SPKMINUS	O	A	-	-	Audio speaker differential output minus.
MIC_IN	I	A	-	-	Microphone single end input.
MIC_P	I	A	-	-	Differential microphone positive input. **Note**: If single end input microphone is used, leave this pin unconnected.
MIC_N	I	A	-	-	Differential microphone negative input. **Note**: If single end input microphone is used, leave this pin unconnected.
AD0	I	A	-	-	A/D input node 1, or providing 3.3V output under software control; connecting to XP (X positive) channel of touch panel.
AD1	I	A	-	-	A/D input node 2, or providing 0V output under software control; connecting to XN (X negative) channel of touch panel.

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
AD2	I	A	-	-	A/D input node 3, or providing 3.3V output under software control; connecting to YP (Y positive) channel of touch panel.
AD3	I	A	-	-	A/D input node 4, or providing 0V output under software control; connecting to YN (Y negative) channel of touch panel.
AIN	I	A	-	-	A general-purpose AD input channel.
BANDGAP	I/O	A	-	-	Reference voltage of 1.4V, connecting to an external 10uF and 0.1uF capacitance.
DC_SW18	I/O	A	-	-	Switch output from DC-DC. A 10uH inductor should be connected between this pin and the pin DC_V18O.
DC_V18O	I/O	A	-	-	300mA output current load potential. It is used for digital 1.8V blocks applications and its voltage can be adjusted from 1.5V to 1.8V. It is recommended to connect a 10uF capacitor between this pin and ground.
LDO_V33A_O	O	A	-	-	3.3V output for analog applications, 300mA output current load potential. The output voltage can be adjusted from 2.7V to 3.3V It is recommended to parallel connect two 2.2uF capacitors between this pin and ground.
LDO_V33D_O	O	A	-	-	3.3V output for digital applications, 300mA output current load potential. The output voltage can be adjusted

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
					from 2.7V to 3.3V It is recommended to parallel connect two 2.2uF capacitors between this pin and ground.
HAVDD_DCAP	I/O	A	-	-	Connected a capacitor(optional)
4. CMOS Image Sensor Interface (12)					
VISCLK	O	D	PPU	I/PU	Programmable frequency from dividing ASIC CLK.
VIVREF	I	D	PPU	I/PU	Vertical sync signal from camera.
VIHREF	I	D	PPU	I/PU	Horizontal sync signal from camera.
VIPCLK	I	D	PPU	I/PU	Pixel clock from camera.
VIPIXEL[7:0]	I	D	VIPIXEL[7:5]: PPU VIPIXEL[4:0]: PPD	[7:5] I/PU [4:0] I/PD	Pixel data, supporting YCbCr4:2:2 format data which is compliant with CCIR601/CCIR656.
5. LCD Display Interface (20)					
#MPU_CS	O	D	-	O	LCD chip select.
MPU_A0	O	D	-	O	Data / command select: Low: command. High: display data.
#MPU_RD	O	D	-	O	Read enable.
#MPU_WR	O	D	-	O	Write enable.
MPU_AD[15:0]	I/O	D	PPU: AD[15:10], AD[7:0]; PPD: AD[9:8];	[15:11] I/PU [10] O/PU [9:8] I/PD [7:0] I/PU	Address/data bus.
6. SDRAM Interface (39)					
#MCS	O	D	-	O	SDRAM chip select.
MCLK	O	D	-	O	Main clock (synchronized with respect to internal clock tree).
MADDR[12:0]	O	D	-	O	Address bus.

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
MDATA[15:0]	I/O	D	PPU	I/PU	Memory data bus.
MBA[1:0]	O	D	-	O	Bank select address, Selecting bank to be activated during row address latch time; or selecting bank for read/write during column address latch time.
MRAS	O	D	-	O	Latching row addresses on the positive going edge of the CLK with RAS low.
MCAS	O	D	-	O	Latching column addresses on the positive going edge of the CLK with CAS low.
#MBE[1:0]	O	D	-	O	Byte enable, active low.[0] controls low byte,[1] controls high byte
#MWR	O	D	-	O	Write enable, active low.
MCKE	O	D	-	O	Clock enable, for SDRAM power saving.
7. Nand Flash Interface (14)					
NFC_data[7:0]	I/O	D	PPU	I/PU	Nand Flash data bus.
#NFC_CE[0]	O	D	-	O	Nand Flash chip enable signal 0.
#NFC_CE[1]	I/O	D	PPU	I/PU	Nand Flash chip enable signal 1.
NFC_ALE	I/O	D	PPD	I/PD	Nand Flash address latch enable.
NFC_CLE	I/O	D	PPD	I/PD	Nand flash command latch enable.
#NFC_WR	I/O	D	PPU	O/PU	Nand flash write enable.
#NFC_RD	I/O	D	-	O	Nand flash read enable.
8. GPIO(31)					
GPIO[31:8] GPIO[6:0]	I/O	D	PPU: GPIO[30:23], GPIO[17:16], GPIO[14:5], GPIO[3]; PPD:	[31] I [30:23] I/PU [22:18] I/PD [17:16]	General input/output ports. **Notes:** ***** Apart from the GPIO[29:28], all the GPIO ports can be used as wake-up ports.

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
			GPIO[22:18], GPIO[15] GPIO[4], GPIO[2]; NO PPU,PPD: GPIO[31], GPIO[1:0]	I/PU [15] I/PD [14] O [13:8],[6:5] I/PU [4] I/PD [3] I/PU [2] I/PD [1:0] I	
9. PWM (1)					
PWM	I/O	D	PPD	I/PD	Pulse-width modulated output signal for PWM.
10.I2S Interface (3)					
I2S_BCLK	I/O	D	PPU	I/PU	I2S bit clock.
I2S_LRCLK	I/O	D	PPU	I/PU	I2S channel selection.
I2S_DIO	I/O	D	PPU	I/PU	I2S serial data input/output.
11. UART/MMC/SPI (16)					
UTD	O	D	PPU	I/PU	Transmit data bit of UART.
URD	I	D	PPU	I/PU	Receive data bit of UART.
MCK	O	D	-	I	MMC/SD operating clock.
MCMD	I/O	D	-	O	MMC/SD command.
MMC_data[7:0]	I/O	D	PPU	I/PU	MMC/SD data bus.
#SPI_CS	I/O	D	PPU	I/PU	SPI chip select, active low.
SPI_CLK	I/O	D	PPD	I/PD	SPI clock.
SPI_MOSI	I/O	D	PPD	I/PD	In host mode, data output; in client mode, data input.
SPI_MISO	I/O	D	PPU	O/PU	In host mode, data input; in client mode, data output.
12. JTAG (5)					
#TRST	I	D	-	I	JTAG logic reset.
TMS	I/O	D	PPU	I/PU	JTAG mode select.

PIN NAME	DIRECTION	ANALOG/ DIGITAL	PULLUP /PULLDOWN	RESET	DESCRIPTION
TCLK	I/O	D	PPU	I/PU	JATG clock, less than 1 MHz, asynchronous with CLK.
TDI	I/O	D	PPU	I/PU	JTAG serial data input.
TDO	I/O	D	PPU	O	JTAG serial output.
13. Scan Control (1)					
SCAN_MODE	I	D	PD	I/PD	Scan mode selection, connecting to LOW for normal operations.
14. Power and Ground (28)					
VDD	PWR	D	-	-	2
VDDIO	PWR	D	-	-	4
VSS	GND	D	-	-	3
VSSIO	GND	D	-	-	5
Vbat(RTC)	PWR	D	-	-	1
AVDD18(PLL)	PWR	A	-	-	PLL voltage, it is recommended to connect a 1uF capacitor and a 0.1uF capacitor parallel between this pin and ground.
AVSS	GND	A	-	-	1
AVDD	PWR	A	-	-	1
VDD33(USB)	PWR	A	-	-	1
VSS(USB)	GND	A	-	-	1
SPVSS	GND	A	-	-	2
SPVDD	PWR	A	-	-	2

Notes:

1. I----INPUT, O----OUTPUT, I/O----INPUT/OUTPUT, PWR----POWER, GND----GROUND, A ---- ANALOG, D----DIGITAL.

2. PU----PULLUP, PD----PULLDOWN: Corresponding ports have been attached pullup/pulldown function.

PPU----PROGRAMMABLE PULLUP, PPD---- PROGRAMMABLE PULLDOWN: The pull-up/pull-down function attached to the corresponding ports is configurable (enabled or disabled) by corresponding registers. Default status is that the pull-up/pull-down function attached to the corresponding port is enabled.

2.2 Shared-Pin List

In order to reduce pin numbers, many pins are shared by two or three function blocks that would not be implemented at the same time. The table below lists the shared pins.

Table 2-2 Shared-Pin List

MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	RESET STATE
Nand Flash	NFC_data[0]	LCD	MPU_AD[0]	MMC/SD	MMC_data[0]	NFC_data[0]
Nand Flash	NFC_data[1]	LCD	MPU_AD[1]	MMC/SD	MMC_data[1]	NFC_data[1]
Nand Flash	NFC_data[2]	LCD	MPU_AD[2]	MMC/SD	MMC_data[2]	NFC_data[2]
Nand Flash	NFC_data[3]	LCD	MPU_AD[3]	MMC/SD	MMC_data[3]	NFC_data[3]
Nand Flash	NFC_data[4]	LCD	MPU_AD[4]	MMC/SD	MMC_data[4]	NFC_data[4]
Nand Flash	NFC_data[5]	LCD	MPU_AD[5]	MMC/SD	MMC_data[5]	NFC_data[5]
Nand Flash	NFC_data[6]	LCD	MPU_AD[6]	MMC/SD	MMC_data[6]	NFC_data[6]
Nand Flash	NFC_data[7]	LCD	MPU_AD[7]	MMC/SD	MMC_data[7]	NFC_data[7]
GPIO	GPIO[30]	Nand Flash	#NFC_CE[1]	-	-	GPIO[30]
Nand Flash	NFC_CLE	LCD	MPU_AD[8]	SPI	SPI_MOSI	NFC_CLE
Nand Flash	NFC_ALE	LCD	MPU_AD[9]	SPI	SPI_CLK	NFC_ALE
Nand Flash	#NFC_WR	LCD	MPU_AD[10]	SPI	SPI_MISO	#NFC_WR
Nand Flash	#NFC_RD	MMC/SD	MCMD	-	-	#NFC_RD
GPIO	GPIO[31]	MMC/SD	MCK	-	-	GPIO[31]
GPIO	GPIO[25]	LCD	MPU_AD[11]	-	-	GPIO[25]
GPIO	GPIO[26]	LCD	MPU_AD[12]	-	-	GPIO[26]
GPIO	GPIO[27]	LCD	MPU_AD[13]	-	-	GPIO[27]
GPIO	GPIO[28]	LCD	MPU_AD[14]	-	-	GPIO[28]
GPIO	GPIO[29]	LCD	MPU_AD[15]	-	-	GPIO[29]
GPIO	GPIO[3]	Camera	VIPIXEL[6]	Reset and clock	Watch_dog	GPIO[3]
GPIO	GPIO[4]	PWM	PWM	-	-	GPIO[4]
GPIO	GPIO[5]	Camera	VIVREF	-	-	GPIO[5]

MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	RESET STATE
GPIO	GPIO[6]	SPI	#SPI_CS	-	-	GPIO[6]
GPIO	GPIO[8]	Camera	VIHREF			GPIO[8]
GPIO	GPIO[9]	UART	URD	-	-	GPIO[9]
GPIO	GPIO[10]	UART	UTD	-	-	GPIO[10]
JTAG	TCLK	I2S	I2S_BCLK	GPIO	GPIO[11]	TCLK
JTAG	TMS	I2S	I2S_LRCLK	GPIO	GPIO[12]	TMS
JTAG	TDI	I2S	I2S_DIO	GPIO	GPIO[13]	TDI
JTAG	TDO	Reset and clock	PCLK_out	GPIO	GPIO[14]	TDO
GPIO	GPIO[16]	Camera	VIPIXEL[7]	-	-	GPIO[16]
GPIO	GPIO[17]	Camera	VIPIXEL[5]	-	-	GPIO[17]
GPIO	GPIO[18]	Camera	VIPIXEL[4]	-	-	GPIO[18]
GPIO	GPIO[19]	Camera	VIPIXEL[3]	-	-	GPIO[19]
GPIO	GPIO[20]	Camera	VIPIXEL[2]	-	-	GPIO[20]
GPIO	GPIO[21]	Camera	VIPIXEL[1]	-	-	GPIO[21]
GPIO	GPIO[22]	Camera	VIPIXEL[0]	-	-	GPIO[22]
GPIO	GPIO[23]	Camera	VISCLK	-	-	GPIO[23]
GPIO	GPIO[24]	Camera	VIPCLK	-	-	GPIO[24]

3 Functional Description

3.1 PMU

The power management unit, consisting of a step-down DC/DC regulator (BUCK18) and a LDO (LDO33), governing power functions of the AK3671 processor, is responsible for coordinating many functions, including:

- providing power to integrated circuits (both analog circuits and digital circuits)
- monitoring power connections

3.1.1 LDO and DC/DC Regulator

The embedded low-dropout regulator is used to power the internal analog circuits and digital circuits. The LDO provides 200mA output current and over-current protection.

Promising an efficiency of 83 percent, the step-down DC/DC regulator operates at 1000KHz and accepts voltage supply between 3V and 5V.

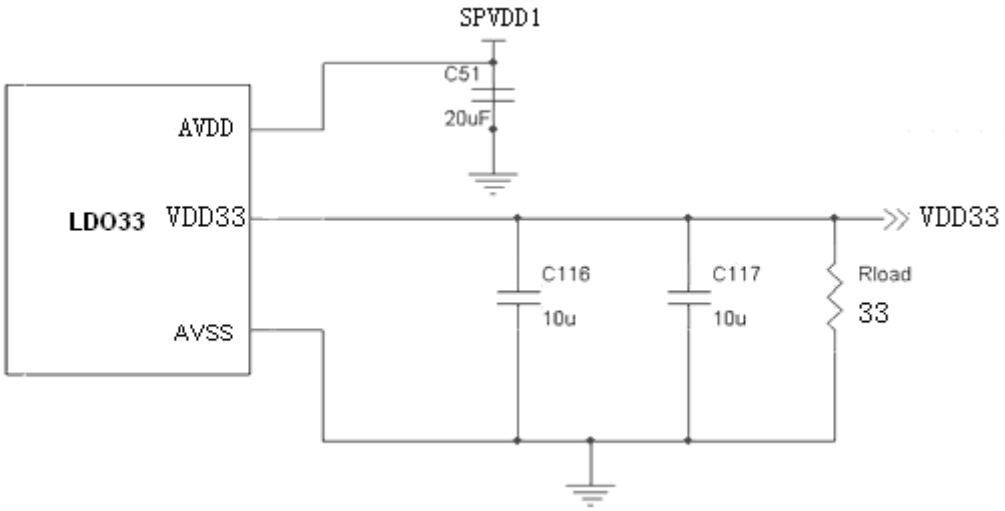


Figure 3-1 Typical Application of LDO33

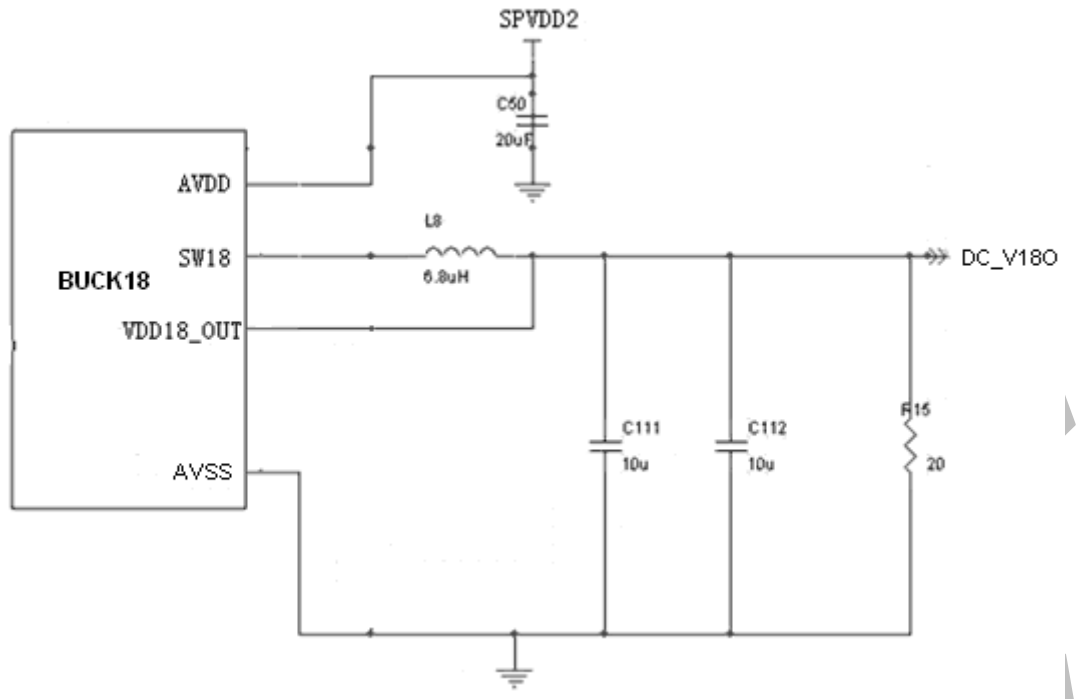


Figure 3-2 Typical Application of BUCK18

Table 3-1 Electrical Characteristics of LDO33

Condition: Unless otherwise noted, Vin=3.7V, T=27℃, Cout = 4.7uF, ESR = 50mOhm.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vin	Input voltage	-	3.5	3.8	5	V
Vout (accuracy)	Output voltage	Default	-3	-	+3	%
Vout	Output voltage	-	-	3.3	-	V
Iout	Output current	-	-	-	200	mA
△Vout,	Load regulation	T=27 ℃, Vin=3.3V,	-	40	-	mV
△Vout/△Iout		@Iout=1 to 100mA		340	-	mOhm
△Vout,	Line regulation	Iout=1mA	-	2	-	mV
		@Vin=3.3V to 5V	-	0.2	-	%
△Vout/△Vin		Iout=100mA(MAX)	-	6	-	mV
		@Vin=3.0V to 5V	-	0.5	-	%
Icc	Vin Quiescent Current	No load	-	50	-	uA
Ipd	Power-down	-	-	0.1	-	uA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	current					

Note: Load Transient Response settle-up time tolerances 0.1% difference of final Vout value.

Table 3-2 Electrical Characteristics of DC/DC

Condition: Unless otherwise noted, typical values are at T_A = +27°C and all Current Values are dynamic.

SYMBOL	PARAMETER	CONDITION	TYP.	UNIT
V_{IN}	Operating Supply Voltage	I_{LOAD_max}=200mA	3~5	V
V_{OUT}	Output Voltage	0mA<I_{LOAD}<200mA	1.5~1.8	V
I_{LOAD_MAX}	MAX Output Current	3.0V<V_{IN}<5.0V	200	mA
I_{ON_LOAD}	Vin Quiescent Current	I_{LOAD} = 0mA	<150	uA
$I_{powerdown}$	Vin Shutdown Current	27°C	<1	uA
V_{ripple}	Output Voltage Ripple	I_{LOAD}=100mA,ESR<40mΩ	<40	mV
η	Efficiency	I_{LOAD}=80mA	83	%
$OSC_{Frequence}$	OSC Frequency	27°C	1000	kHz
I_{Limit}	Peak Current Limit	27°C	700	mA
Rpswitch	P-Channel On-Resistance	VIN=3.8V	500	mΩ
Rnswitch	N-Channel On-Resistance	VIN=3.8V	500	mΩ

3.1.2 Typical Power-On Time

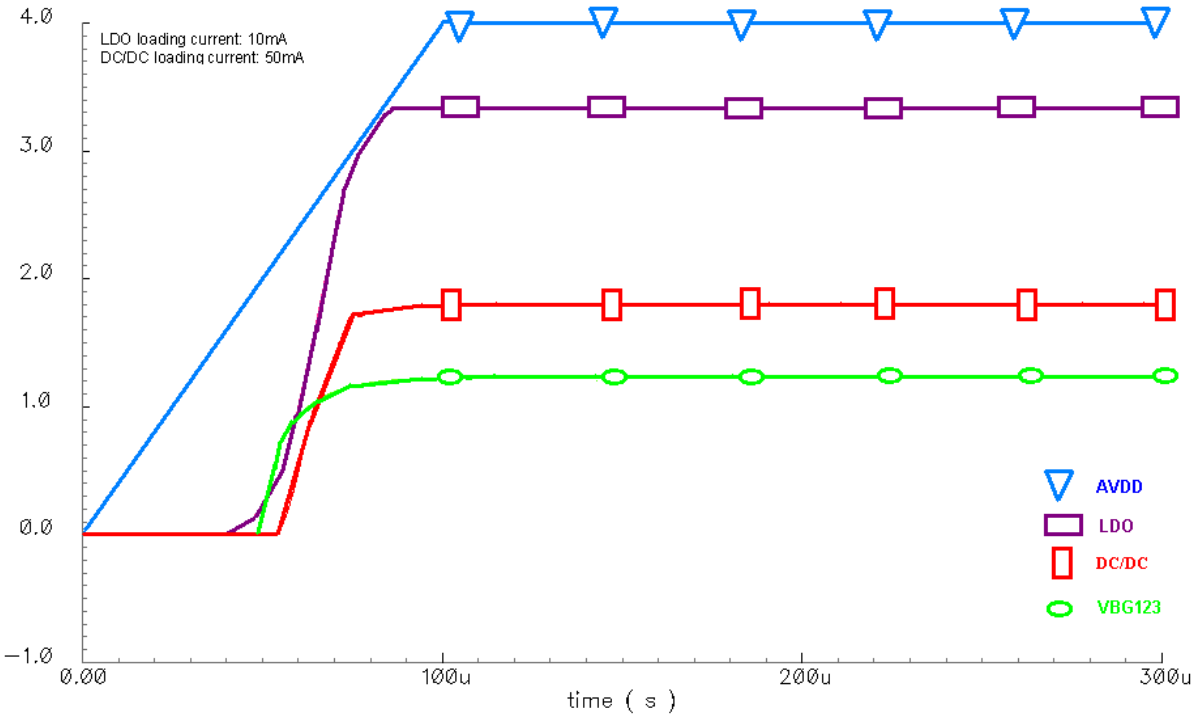


Figure 3-3 Power-On Time

3.1.3 Temperature Detector

The temperature detector monitors the processor's temperature, and generates an interrupt to the CPU core when the temperature is beyond the allowable temperature range. As shown in Figure 3-4, when the temperature is rising, if the temperature reaches 140^0C, an interrupt will be generated; and when the temperature is falling, if the temperature is below 120^0C, an interrupt will be generated too.

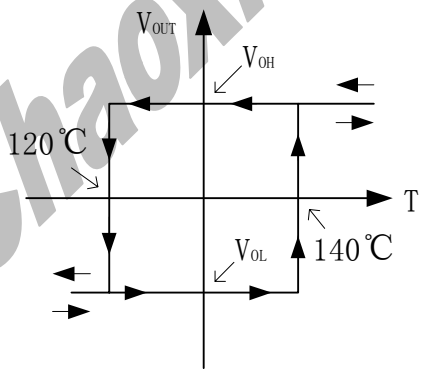


Figure 3-4 Temperature Status

3.2 System Control

3.2.1 Clock Generation and Control

Figure 3-5 illustrates the internal clock generation and control of the AK3671 processor. In normal operation, the AK3671 accepts two possible crystals: 32.768KHz and 12MHz. The former is input from the pin XTAL32KI and generates a precise clock for the RTC module; while the latter is input from the pin XTAL12MI and generates working clocks for all the modules with the exception of RTC.

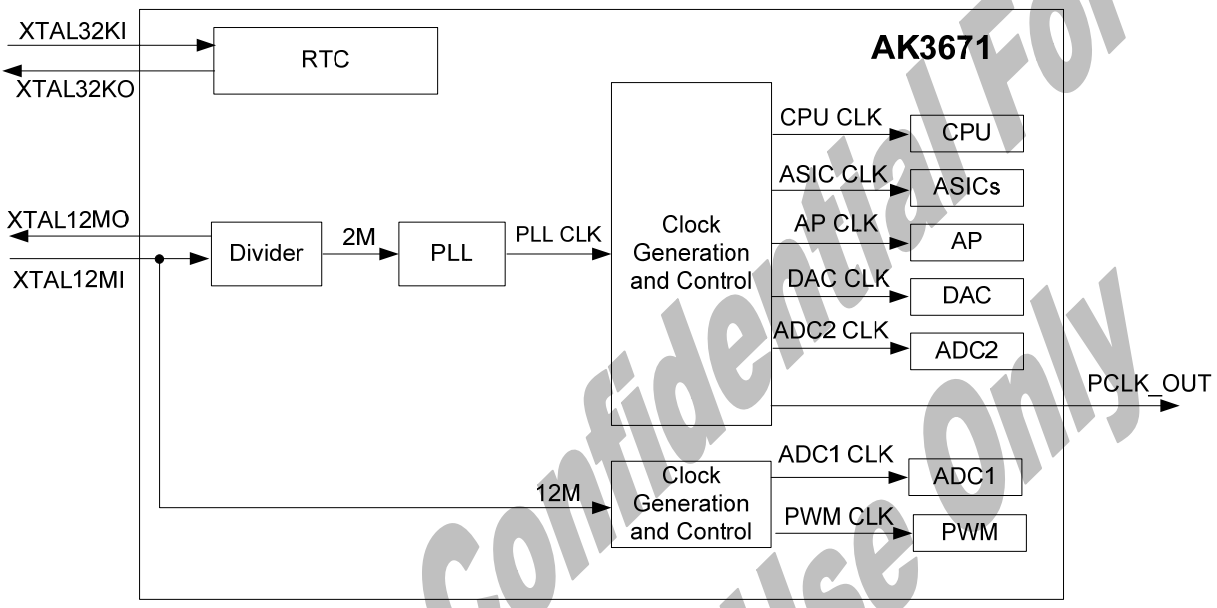


Figure 3-5 Clock Generation and Control

Notes:

1. CPU CLK is the working frequency of CPU core. It may be equal to ASIC CLK or twice of the ASIC CLK.
2. ASICs refer to all the functional blocks with the exception of CPU core, audio processor, I2S master and slave interfaces, ADCs and DACs. The ASIC CLK just provides a clock to the ASICs. The working frequency for a given functional block is programmable.
3. AP CLK provides working frequency to audio processor and I2S slave interface.
4. DAC CLK provides working frequency to DACs and I2S master interface.
5. ADC1 CLK is the working frequency of the ADC used for touch screen and battery measurement.
6. ADC2 CLK is the working frequency of the ADC used for voice recording.
7. PCLK_OUT is a programmable clock output.

8. PWM CLK provides working clock to PWM.

9. PLL can be powered down when the system is in standby mode or power down mode. Then the CPU CLK, ASIC CLK, AP CLK, ADC2 CLK, DAC CLK and PCLK_out are off.

10. The external connection of the pins XTAL32KI and XTAL32KO is quite strict. Figure 3-6 gives a typical connection; and Table 3-3 recommends the values of critical parameters.

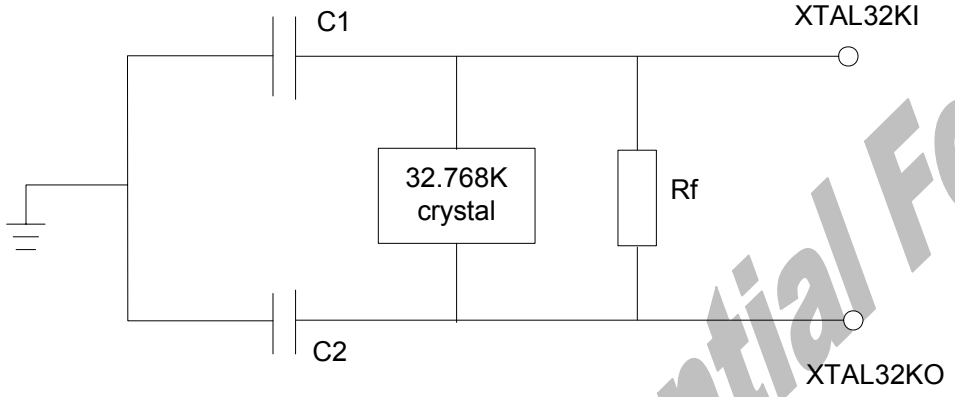


Figure 3-6 A Typical Connection Between XTAL32KI and XTAL32KO

Table 3-3 Recommended Parameters

ITEM	MIN	TYP	MAX	UNIT
Rf	1	2	3	M ohm
C1	25	30	40	pF
C2	25	30	40	pF

All the clocks mentioned above are configurable by software and the relationships with PLL CLK are as follows:

Table 3-4 Main Clock and Internal Clocks

ITEM	RELATIONSHIP WITH PLL CLOCK	NOTE
PLL CLK	When the system is reset, PLL CLK is set to 120MHz by default.	Ranging from 120MHz to 184MHz, PLL CLK is configurable with step length of 4MHz.
ASIC CLK	ASIC CLK = $\frac{PLLCLK}{2^n}$ (n=1,2, …,7)	-

ITEM	RELATIONSHIP WITH PLL CLOCK	NOTE
CPU CLK	CPU CLK = ASIC CLK or CPU CLK = 2 X ASIC CLK	Under software control, CPU CLK can be equal to ASIC CLK or twice of the ASIC CLK.
AP CLK	AP CLK = $\frac{PLLCLK}{2^n}$ (n=1,2, …,7)	AP CLK must be faster than or equal to ASIC CLK.
PCLK_out	PCLK_out = $\frac{PLLCLK}{N}$ (N=2, 3,…,2^7)	When the system is reset, the pin PCLK_OUT outputs a clock that is equal to $\frac{mainclk}{128}$. Software may disable the clock output if such clock is not needed.
ADC1 CLK	ADC1 CLK = $\frac{12M}{N+1}$ (N=0, 1,…,2^4)	Recommended value is 4MHz.
ADC2 CLK	ADC2 CLK = $\frac{PLLCLK}{N+1}$ (N=0,1, …,2^7)	-
DAC CLK	DAC CLK = $\frac{PLLCLK}{N+1}$ (N=0,1, 2,…,2^6)	DAC CLK is recommended to range from 10MHz to 18MHz.

3.2.2 Reset Module

The #RST signal, when asserted low, puts all internal states (with the exception of RTC module) into predefined values. Figure 3-7 shows the reset timing of AK3671.

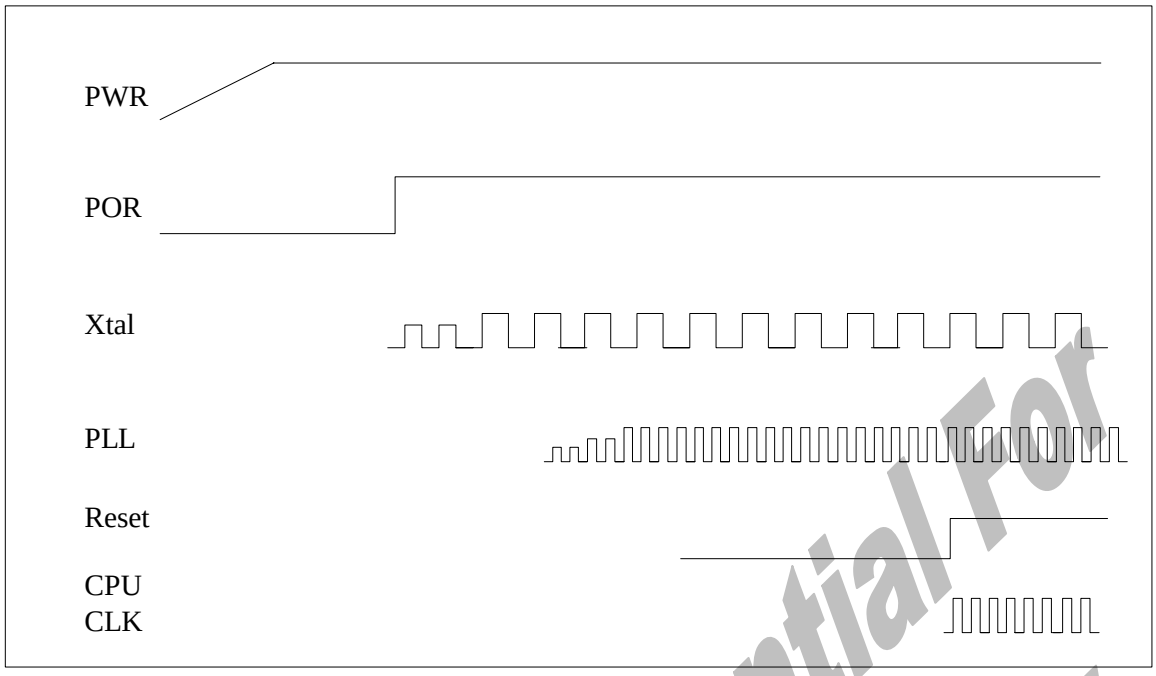


Figure 3-7 AK3671 Power On Reset Timing

Excluding PWM module, all modules contained in the AK3671 processor can be reset independently by software.

3.2.3 Interrupt Module

The interrupt module collects interrupt requests from the ASICs and provides an interface to the CPU core. The CPU responds to the interrupts according to two principles:

1) priority, if multiple interrupt requests are sent at the same time;

The interrupt module supports both fast and normal interrupts, and of course the fast interrupts get the higher priority.

2) whether the interrupt has been masked or not.

The interrupt module can mask/unmask every interrupt source of normal and fast interrupts with specific bit of mask registers. Only the interrupt requests from unmasked interrupt source are responded.

The ASIC continually sends the interrupt request until it is informed by software that its request has been responded. Besides, it should be noted that when an ASIC interrupt is being processed, the interrupt is masked until the interrupt process has been finished. That is,

AK3671 cannot respond to two interrupts concurrently even though the interrupts are requested by the same ASIC.

3.2.4 Bootstrap Module

When the AK3671 processor is reset, all ASIC units except GPIOs, UART, and JTAG are disabled, and the CPU core gets its first instruction from address 32'0x0000, 0000, which belongs to the on-chip ROM address space. It first reads the value of GPIO[4] to judge the boot up mode. If GPIO[4] is asserted ("1"), the AK3671 is boot up from USB port; if GPIO[4] is de-asserted ("0"), the AK3671 reads data from Nand Flash and Serial Flash in succession, and checks the password. If the password is matched, AK3671 is boot up from Nand Flash or Serial Flash. If not, AK3671 is boot up from Mass Storage.

Note: GPIO[4] can be used as a general purpose output port after the system has been booted up from USB port.

3.2.5 Power Management

AK3671 implements a simple and powerful power control mechanism, unit clock enable. During normal operation, only the clock for CPU core and the memory controller is turned on; all ASIC accelerator units are turned off their clock inputs. An accelerator is clocked on only when it is needed, and it is immediately clocked off after its use has been finished. All internal memories are in LOW-POWER state, except when they are accessed.

3.2.6 Working Modes

There are three working modes for the AK3671 processor:

1) **Normal operating**

All the functional blocks are clocked on/off in accordance with specific operating requirement.

2) **Standby**

The RTC module is clocked on, PLL is powered down and other modules (including CPU core) are clocked off.

3) **Power down**

The RTC module is powered on, and other modules (including CPU core) are powered down.

3.2.7 JTAG

JTAG is AK3671's major software debugging tool. The JTAG of AK3671 supports breakpoints, controlling, monitoring and real-time running otherwise.

3.3 RTC Module

The RTC module accepts solely the working clock from external 32.768KHz crystal. While the system is powered off, it may be driven by the backup battery that supplies power through the pin Vbat (RTC).

The RTC module provides following functions::

- real-time clock
- alarms or wake-up signals in standby mode
- alarms in power down mode
- interrupts in normal operating mode
- a RTC watchdog timer

An alarm or an interrupt may be set by accessing corresponding registers and loading the exact time that the alarm/interrupt should be generated.

The AK3671 processor can be woken up on one of the following two conditions:

1. 32.768KHz clock alarm time is met
2. wake-up signal width >10 ASIC CLKs

Notes:

1) Apart from GPIO[29:28], all the GPIO ports can be used as wake-up ports;
2) Wakup signal may be high active or low active.

3.4 CPU core

The 32-bit RISC microprocessor core is designed specifically for high performance, cost-effective and low power applications.

The CPU core provides following features:

- Integrated ALU (Arithmetic Logic Unit) and MAC(multiply-accumulate)
- 5-stage execution pipeline
- Combined 8KB instruction and data cache
- Memory Management Unit (MMU) for multi-tasking software
- Advanced High-performance Bus (AHB) external interface

- JTAG debug

3.5 Memory

3.5.1 On Chip Memory

To improve the AK3671's performance, 16KB ROM is added to for booting the CPU after each reset, and 2KB RAM is included as a scratch memory for high-performance and low-power kernel applications.

3.5.2 External Memory

3.5.2.1 RAM Interface

The RAM controller is the bridge logic that connects an internal unit to the external SDRAM. It provides following features:

- one chip select
- supporting up to 64MB memory
- supporting self-refresh function
- external SDRAM can work at a maximum frequency of 90MHz

Figure 3-8 and Figure 3-9 show the write and read timing diagrams of SDRAM interface.

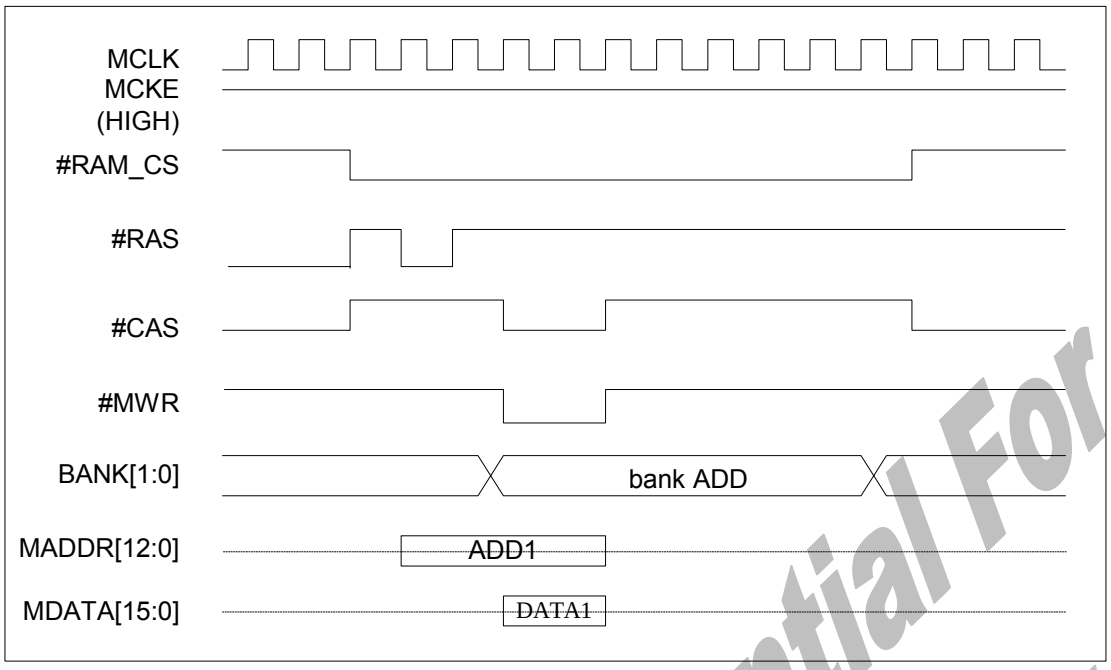


Figure 3-8 Write Timing Diagram of SDRAM Interface

Note: Only MADDR[11:0] are employed for the 8MB/16MB SDRAM.

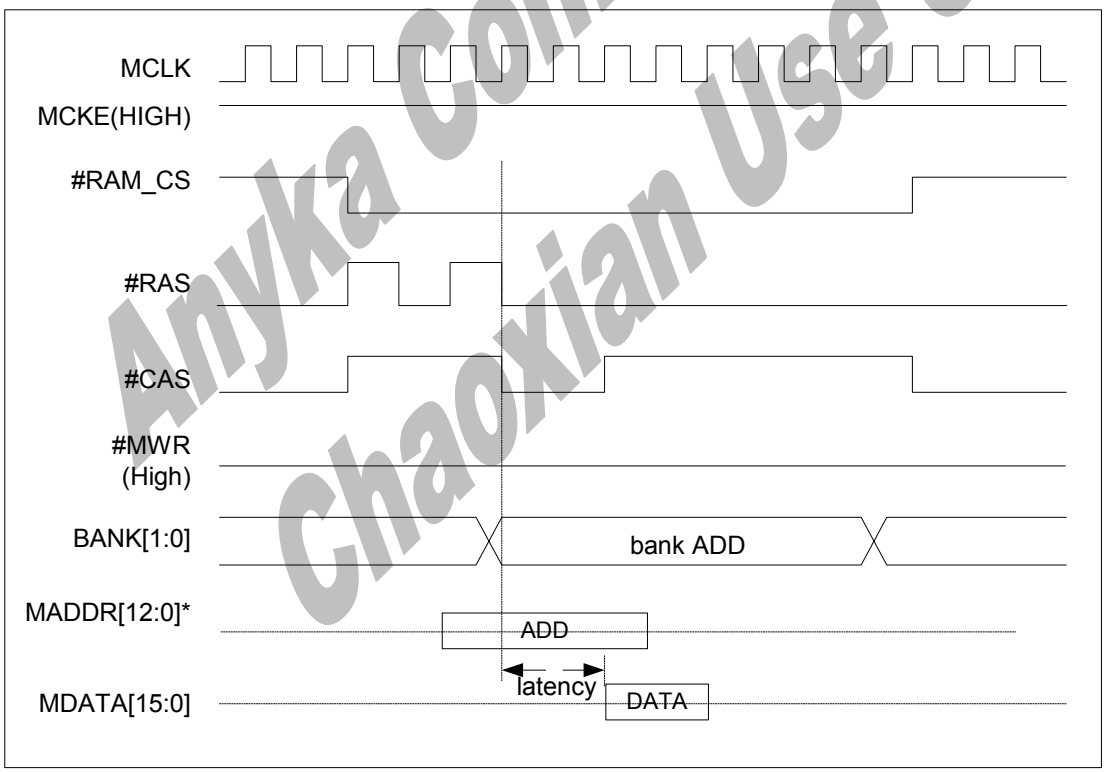


Figure 3-9 Read Timing Diagram of SDRAM Interface

Notes:

1. Latency is the delay between the registration of a READ command and the availability of the first piece of output data. The latency of the SDRAM interface is fixed to 2 MCLK cycles.
2. A read command is valid only when SRAM_CS1 is low, #RAS is high, #CAS is low, and #MWR is high.
3. Only MADDR[11:0] are employed for the 8MB/16MB SDRAM.

3.5.2.2 Nand Flash Interface

The Nand Flash interface can connect up to 2 pieces of 8-bit wide Nand Flash concurrently regardless of Nand Flash's page size, density or organization. It provides ECC function for each piece of Nand Flash, which may be enabled or bypassed by configuring corresponding register(s).

The on-chip ECC module can correct 4/8/12/16/24/32 bits error every data block (maximum 1536B).

Figure 3-10 shows the initial timing of Nand Flash interface, which is configurable by software.

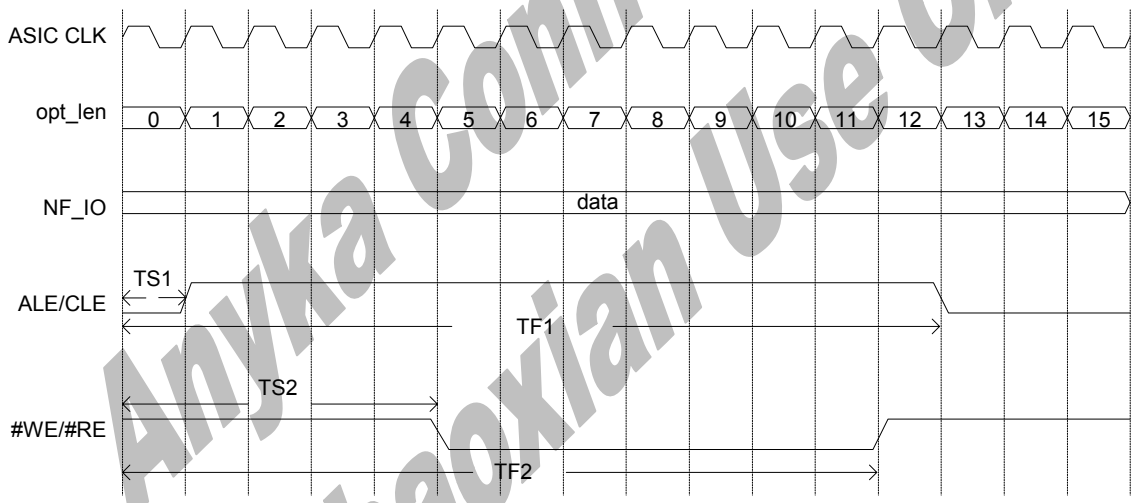


Figure 3-10 Nand Flash Interface Timing

Notes:

1. Opt_len refers to the valid period of an address, a command, or a data read/write operation. It is configurable by four bits of Command Length Register/Data Length Register, thus it ranges from 1 ASIC CLK to 16 ASIC CLKs. The default value is 16 ASIC CLKs, as shown in the figure above.

2. The rising/falling edge of ALE/CLE/#WE in a command operation is configurable respectively by four bits of Command Length Register. The default value of TS1 is “1” (the second ASIC CLK cycle); that of TF1, “13” (the fourteenth ASIC CLK cycle); that of TS2, “5” (the sixth ASIC CLK cycle); and that of TF2, “12” (the thirteenth ASIC CLK cycle).

3. The rising/falling edge of #WE/#RE in a data operation is configurable respectively by four bits of Data Length Register. The default value of TS2 for #WE is “5” (the sixth ASIC CLK cycle); that of TF2 for #WE, “12” (the thirteenth ASIC CLK cycle); that of TS2 for #RE, “5” (the sixth ASIC CLK cycle); and that of TF2 for #RE, “12” (the thirteenth ASIC CLK cycle).

3.6 Advanced High-performance Bus (AHB)

The AHB is a kind of high performance bus for burst data transfer. AK3671 provides two AHB channels: one is for CPU access, and the other is for debug use.

When the CPU wants to access the memory, including SDRAM and registers, it sends AHB commands to the corresponding memory controller. Then the memory controller translates the AHB commands into the signals to its module and generates the memory or register access signals to realize loading or storing data.

AHB write and read timing are fully compliant with *AMBA AHB Protocol.*

3.7 DMA/CRC Accelerator

AK3671 contains two DMA controllers: DMA controller and DMA/CRC controller. The DMA controller transfers data to/from external RAM in response to the requests generated by DMA-capable functional blocks (such as UART, SPI, etc.); while the DMA/CRC controller controls the data transfer with/without CRC between two kinds of external memories. The DMA/CRC controller is seen as a DMA-capable functional block. The data transfer does not begin until the DMA Controller has sent an ACK signal to DMA/CRC controller.

3.8 Register Bus Controller

The register bus controller translates AHB (Advanced High-performance Bus) transactions targeted at register space into simple WRITE and READ pulses. To simplify the interface design with AHB of CPU core, each register access is carried out in minimum 2 clock cycles.

The register bus controller also includes logic to interface with the audio processor module directly, either via audio processor I/O registers or through IDMA.

3.9 Video Processor

The video processor provides hardware acceleration to the compression and decompression of moving pictures and video. It supports MPEG4/H.263/M-JPEG encoding and decoding, which fully comply with *ITU-T Recommendation H.263(02/98), Information technology — Coding of audio-visual objects —Part2: Visual (ISO/IEC 14496-2), and Information Technology—Digital Compression and Coding of Continuous-Tone Still Images Requirements and Guidelines (09/92).* The performance of the video processor is:

- MPEG4 SP. Level 0,1,2&3 codec
- H.263 baseline codec
- Motion JPEG codec

3.9.1 Typical Encoding Application

Figure 3-11 shows a typical application of the video encoding. The data from camera should be compatible with CCIR601 or CCIR656 and is stored temporarily in external RAM. Video processor encodes the data gotten from the external RAM and sends back the encoded bit stream data to the external RAM.

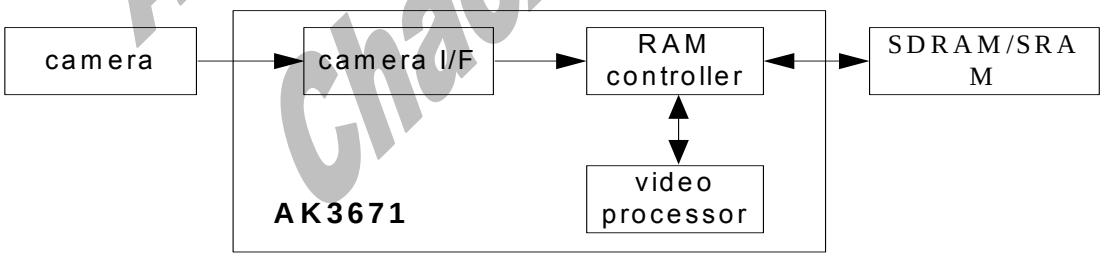


Figure 3-11 A Typical Application of Video Encoding

3.9.2 Typical Decoding Application

A typical application of video decoding is shown in Figure 3-12. The video processor decodes the bit stream data from external RAM and sends back to RAM after decoding. The decoded data is finally sent to LCD for display.

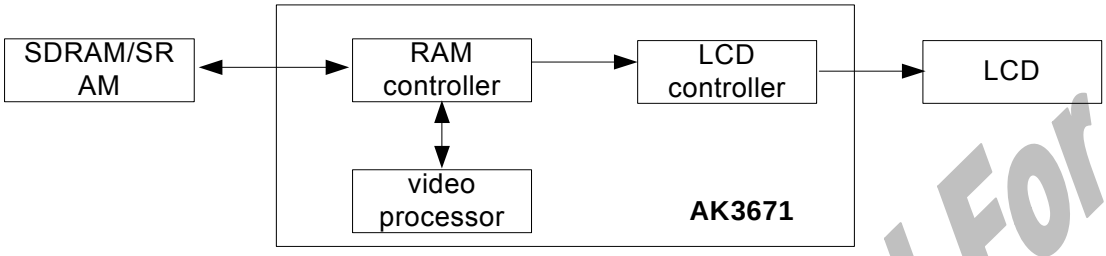


Figure 3-12 A Typical Application of Video Decoding

3.10 Image Processor

The image processor is a JPEG accelerator that off-loads CPU by accelerating the computation-intensive parts (DCT/IDCT, Q/IQ, Huffman, and etc.) of JPEG compression and decompression. It is compatible with *Information Technology—Digital Compression and Coding of Continuous-Tone Still Images Requirements and Guidelines (09/92).*

3.10.1 Typical Encoding Application

Figure 3-13 shows a typical application of the image encoding. The data from camera should be compatible with CCIR601 or CCIR656 and is stored temporarily in external RAM. Image processor encodes the data gotten from external RAM and sends back the encoded data to the external RAM.

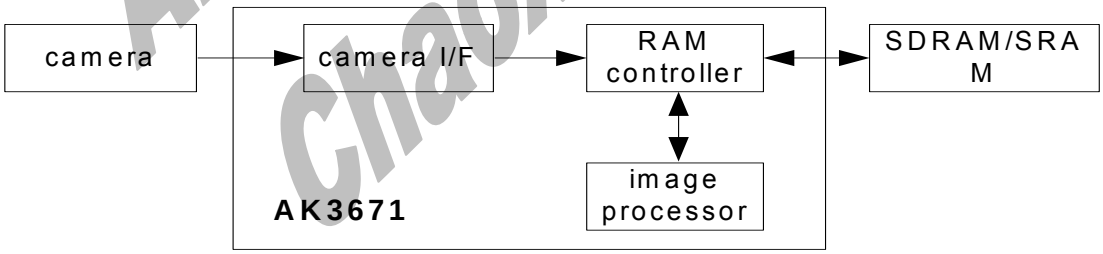


Figure 3-13 A Typical Application of Image Encoding

3.10.2 Typical Decoding Application

A typical application of image decoding is shown in Figure 3-14. The image processor decodes the data from external RAM and sends back to RAM after decoding. The decoded data is finally sent to LCD for display.

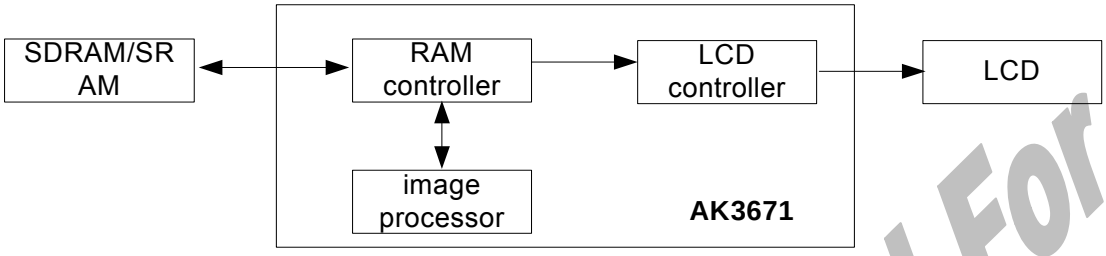


Figure 3-14 A Typical Application of Image Decoding

3.11 Audio Processor

The AK3671 has an embedded audio processor, which has 32KB data cache and 48KB instruction cache. The audio processor running clock (AP CLK) is configurable by corresponding register.

The audio processor supports 64-polyphony MIDI synthesizing compliant with General MIDI 1.0 (GM 1.0) and SP-MIDI, MP3 decoding (full modes), Microsoft's WMA decoding, real-time speech codec (all modes of AMR), AAC/AAC+ decoding, and real-time audio stream in PCM or ADPCM format.

3.11.1 Typical Encoding Application

Figure 3-15 illustrates the process of typical encoding applications, such as voice recording, line in recording, and etc. Input through the microphone interface that contains a PGA, the data is sent to ADC2 and audio processor in succession. The encoded data is stored temporarily in external RAM.

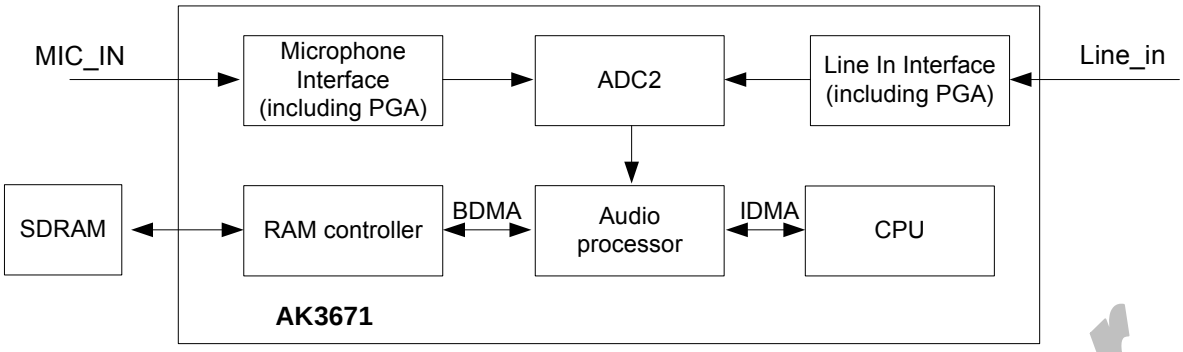


Figure 3-15 Typical Encoding Applications

Notes:

1. *MIC_IN* and *Line_in* are external pins.
2. Please refer to audio analog components section for the details on microphone interface, line in interface and ADC2.

3.11.2 Typical Decoding Application

Figure 3-16 illustrates the typical process of decoding applications, such as MP3/MIDI/WMA playing. The data stored in MMC/SD/Nand Flash or other medium is sent to external RAM first, then to audio processor and DACs, and finally to speaker or headphone.

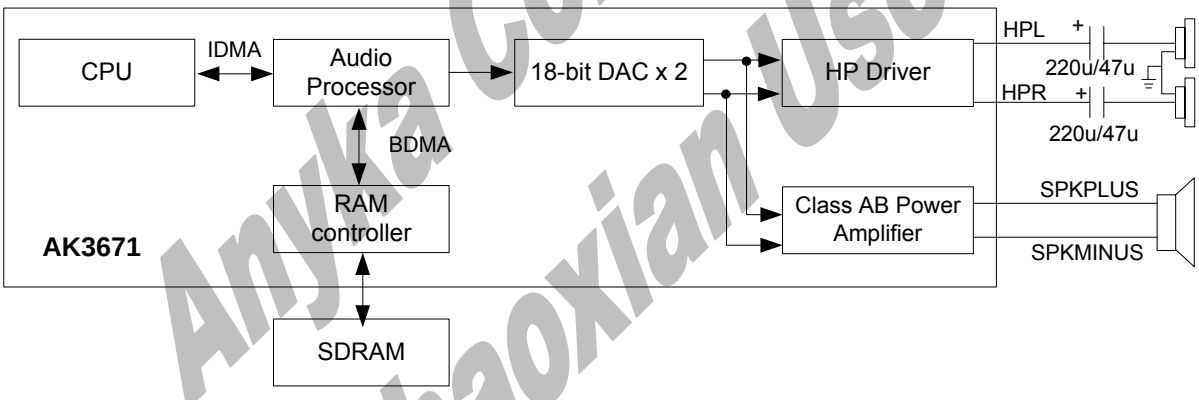


Figure 3-16 A Typical Decoding Application

Note: Please refer to audio analog components section for details on HP driver and Class AB Power Amplifier.

3.12 I2S Interface

I2S is a popular 3-wire serial bus standard protocol developed by Philips Corporation for transmission of 2 channel (stereo) Pulse Code Modulation digital data, where each audio sample is sent MSB first.

The I2S interface supports three kinds of working modes:

1) I2S transmitter master mode

In this mode, the AK3671 provides the BCLK and LRCLK signals and outputs the data from audio processor to the external DAC via the I2S interface. The word length ranges from 3 bits to 24 bits, which is configured by SPORT0 of audio processor.

2) I2S transmitter slave mode

In this mode, the AK3671 accepts the BCLK and LRCLK signals and outputs the data from audio processor to the external DAC via the I2S interface. The word length ranges from 3 bits to 24 bits, which is configured by SPORT0 of audio processor. If the word length of external DAC is more than 24 bits, 0s are added to the end of LSB.

3) I2S receiver slave mode

In this mode, the AK3671 accepts the BCLK signal, LRCLK signal and the data from external ADC via the I2S interface. The word length ranges from 3 bits to 16 bits, which is configured by SPORT1 of audio processor. If the word length of external ADC is more than 16 bits, the LSBs are ignored.

The I2S interface contains four pins, all of which are shared with GPIOs and JTAG.

Table 3-5 I2S Interface

PIN	PULLUP/ PULLDOWN	DESCRIPTION	SHARED WITH	TYPE		
				I2S transmitter master	I2S transmitter slave	I2S receiver slave
I2S_BCLK	PPU	I2S bit clock.	TCLK/ GPIO[11]	O	I	I
I2S_LRCLK	PPU	I2S channel selection.	TMS/ GPIO[12]	O	I	I
I2S_DIO	PPU	I2S serial data input/output.	TDI/ GPIO[13]	O	O	I

PIN	PULLUP/ PULLDOWN	DESCRIPTION	SHARED WITH	TYPE		
				I2S transmitter master	I2S transmitter slave	I2S receiver slave
PCLK_out	PPU	A programmable clock output, controlled by Clock Divider Register.	TDO/ GPIO[14]	O	O	O

Note: PPU: Programmable Pullup (The word “programmable” means that the pull-up function attached to the corresponding ports is configurable (enabled or disabled) by corresponding registers. Default status is that the pull-up/pull-down function attached to the corresponding port is enabled.)

3.12.1 Timing

The I2S interface of the AK3671 processor supports I2S standard waveform.

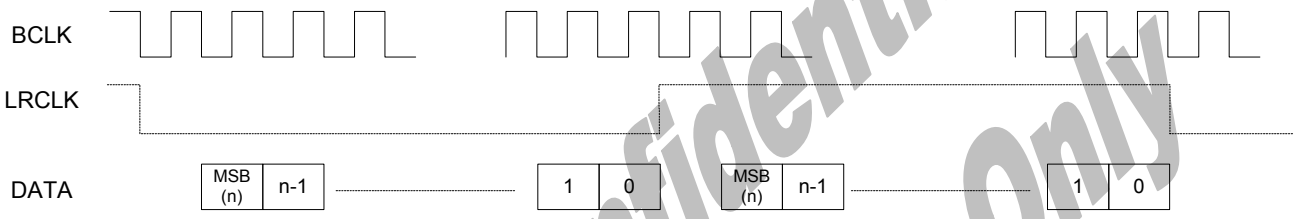


Figure 3-17 I2S Interface Timing

3.12.2 Typical Applications

3.12.2.1 Transmitter modes

When I2S interface works in transmitter master mode or transmitter slave mode, I2S interface is the bridge connecting internal audio processor and off-chip DAC(s).

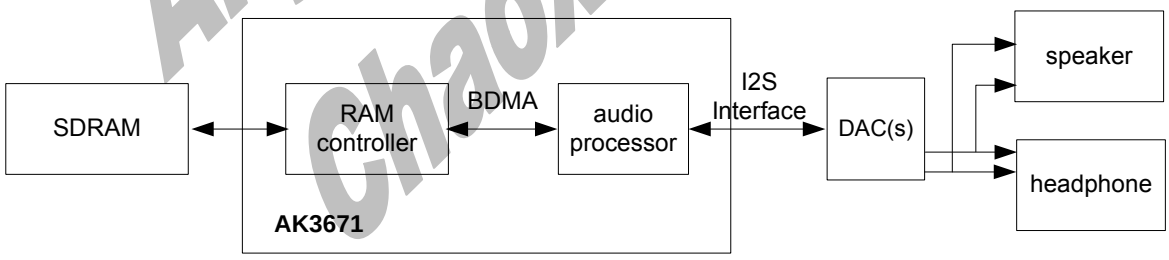


Figure 3-18 Typical Application of I2S Transmitter Modes

3.12.2.2 Receiver Mode

When I2S interface works in receiver slave mode, I2S interface is the bridge connecting internal audio processor and off-chip ADC.

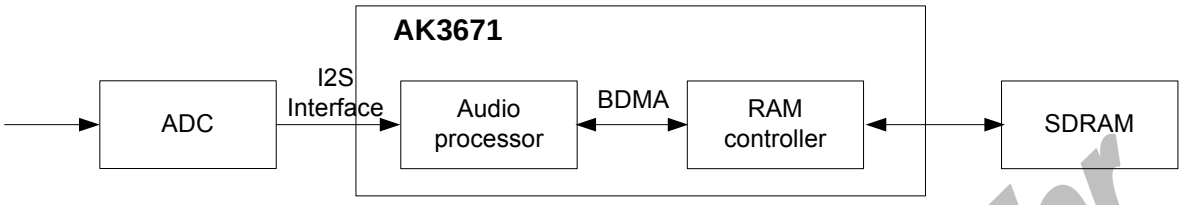


Figure 3-19 Typical Application of I2S Receiver Modes

3.13 Software I2C

I2C bus is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection between devices.

The I2C of the AK3671 processor is simulated by software and implemented by GPIO[0] and GPIO[1].

Table 3-6 I2C Signal Description

SIGNAL NAME	INPUT/OUTPUT	DESCRIPTION	IMPLEMENTED BY
SDA	Bi-directional	Serial Data	GPIO[1]
SCL	Bi-directional	Serial Clock	GPIO[0]

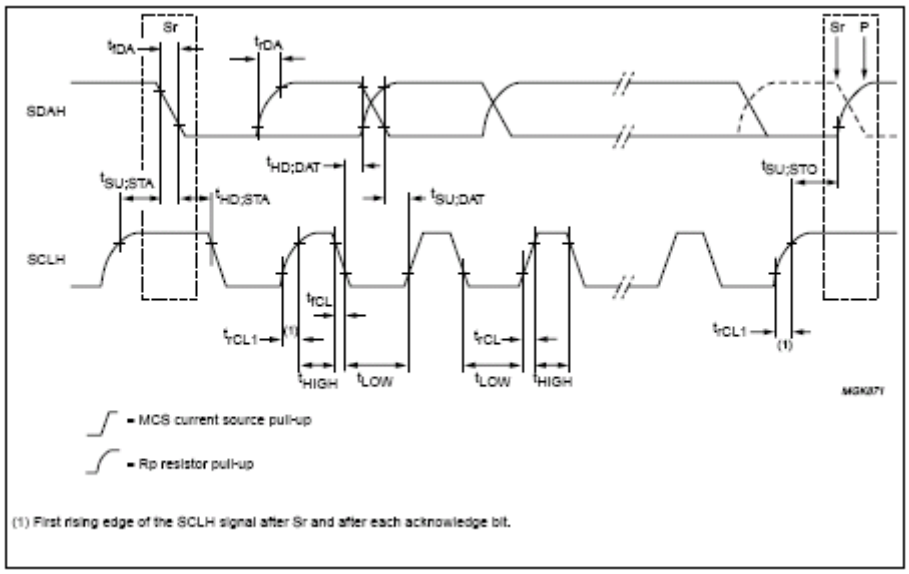


Figure 3-20 I2C bus Timing

Note: Please refer to *The I2C Bus Specification* for I2C configuration.

3.14 Camera Interface

The camera interface acquires data and control signals from the external image sensor, performs data format conversion, shrinks the data, and routes the data to memory.

The features of camera interface are as follows:

- compatible with CCIR 601 and CCIR 656
- supporting CMOS digital camera
- 8-bit YCbCr 4:2:2 format color video/image input data, YCbCr vectors should be in the order of Cb, Y, Cr, Y, Cb, Y, Cr, Y
- user programmable video/image resolutions
- arbitrary ratio image down scaling of M/N where M and N are values from 16 to 1024
- supporting contrast enhancement
- maximum frame refresh rate is half the external CMOS Image Sensor output frame refresh rate
- the external image sensor should be configured to work in Progressive Scan Mode

3.14.1 Timing

3.14.1.1 External Image Sensors Compatible With CCIR 601

The camera interface should accept VIVREF and VIHREF signals from the external CMOS sensor compatible with CCIR 601. VIVREF is an active low input signal indicating that active video line is being transmitted on the video input data bus. VIHREF is an active high input signal indicating that active pixel data is being transmitted on the video input data bus data[7:0]. Figure 3-21 shows the timing of camera interface.

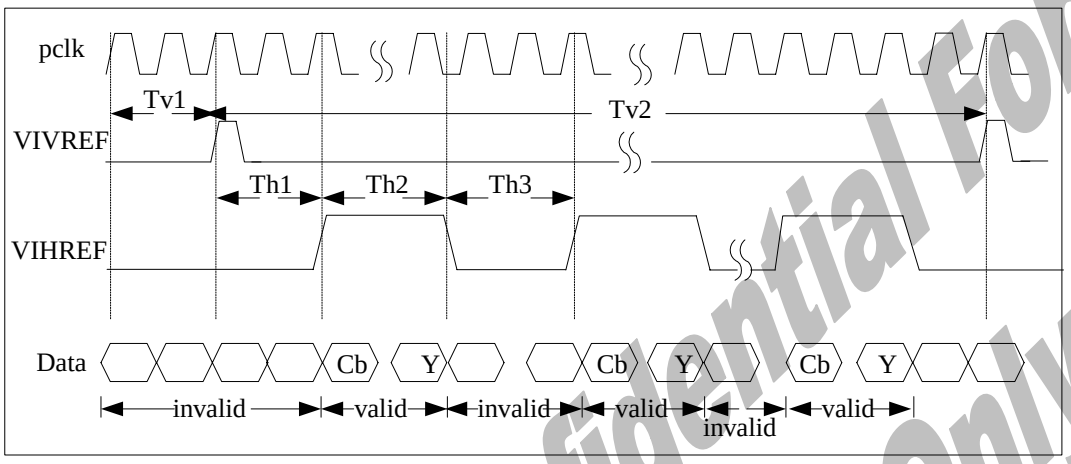


Figure 3-21 Video/Image Input Data line Timing

Notes:

1. Valid data should be in the order of Cb, Y, Cr, Y, Cb, Y, Cr, Y.
2. PCLK, provided with the 8-bit YCbCr 4:2:2 video/image data, is an “interface clock” running at twice the pixel rate.
3. Tv1, Tv2, Th1, Th2, Th3 are configurable by external CMOS image sensor.

3.14.1.2 External Image Sensors Compatible With CCIR 656

The greatest difference between CCIR601 protocol and CCIR656 protocol is that the CMOS image sensors compatible with CCIR656 protocol embed timing reference signals in the data stream. AK3671 processor supports both odd filed timing reference code and even field timing reference code.

Assume that the external CMOS image sensor has been programmed to provide YCbCr 4:2:2 video/image of 526 scan lines per frame, 780 pixel clocks per line. Among the 780x526 frame array, active image is 640x480, i.e. 480 active lines and 640 active pixels per active line, as shown in Figure 3-22.

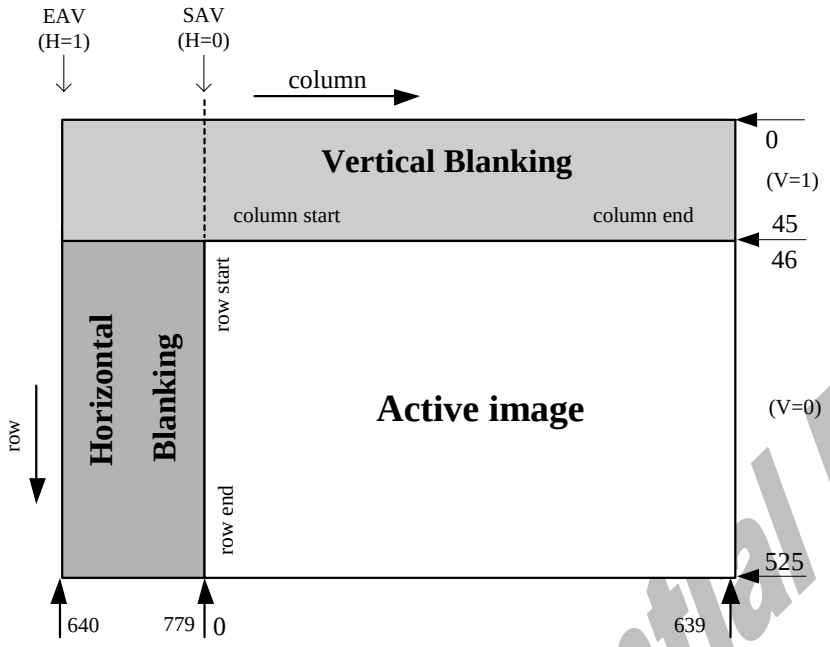


Figure 3-22 Horizontal and Vertical Timing States of Image/Video Compliant With CCIR656 Protocol In Progressive Scan Mode (640x480 resolution)

Notes:

1. EAV and SAV, occurring on every scan line, are digital synchronizing signals indicating the End of Active Pixel and Start of Active Pixel respectively.
2. V and H are timing reference bits. Please see details in Table 3-8.

PCLK, provided with the 8-bit YCbCr 4:2:2 video/image data to sample the YCbCr video data bus with its rising edge, runs at twice the pixel rate. So each scan line (including 780 pixels) should has 1560 interface clock intervals. 1280 intervals, from Interval 0 to Interval 1279, are luminance and chrominance values (640 luminance Y, 320 chrominance Cb, and 320 chrominance Cr values); 8 intervals, from Interval 1280 to Interval 1283, from Interval 1556 to Interval 1559, are synchronizing information; and the rest 272 intervals are invalid data. Table 3-7 defines the 1560 samples of a single scan line of video.

Table 3-6 Detail of A Scan Lind for a 640 x 480 Image

INTERVAL NO.	DATA CONTENT	PIXEL NO.	NOTE
1280	1111 1111	640	EAV
1281	0000 0000		EAV
1282	0000 0000	641	EAV

INTERVAL NO.	DATA CONTENT	PIXEL NO.	NOTE
1283	10V1 P3P2P1P0/ 11V1P3P2P1P0		EAV
1284	1000 0000	642	From 642 to 777, Cb=Cr=80h,Y=10h
1285	0001 0000		
1286	1000 0000	643	
1287	0001 0000		
...	...	...	
1552	1000 0000	776	
1553	0001 0000		
1554	1000 0000	777	
1555	0001 0000		
1556	1111 1111	778	SAV
1557	0000 0000		SAV
1558	0000 0000	779	SAV
1559	10V0 P3P2P1P0/ 11V0P3P2P1P0		SAV
0	U0	0	Start of active pixel
1	Y0		For blanking line 0 to 45,Cb=Cr=80hY=10h
2	V1	1	
3	Y1		
4	U2	2	
5	Y2		
6	V3	3	
7	Y3		
...	...	...	
1272	U636	636	
1273	Y636		
1274	V637	637	
1275	Y637		
1276	U638	638	
1277	Y638		

INTERVAL NO.	DATA CONTENT	PIXEL NO.	NOTE
1278	V639	639	
1279	Y639		End of active pixel

Table 3-7 EAV and SAV Timing Reference Signals

	VALUE(BINARY)	DESCRIPTION
first byte	1111 1111	Fixed for both EAV and SAV
second byte	0000 0000	Fixed for both EAV and SAV
third byte	0000 0000	Fixed for both EAV and SAV
fourth byte	10VH P3P2P1P0 / 11VH P3P2P1P0	V=0 during Active Video V=1 during Vertical Blanking H=0 at the start of Active Video H=1 at the end of Active Video

The first three words of SAV and EAV are preamble, followed by the fourth word indicating start/end of active video or horizontal/vertical blanking area. Hence, the fourth byte 10VHP3P2P1P0B/ 11VHP3P2P1P0B is of vital importance, especially V (Bit[5]) and H (Bit[4]). In order to reduce the probability of error occurring, CCIR656 protocol has defined the lower fourth bits in every case. Not only V (Bit[5]) and H (Bit[4]), but also the lower four bits should be taken into consideration when data stream is received. Table 3-9 and Table 3-10 define the value of the fourth byte in every case.

Table 3-8 The Value of Fourth Byte In Every Case (Odd Field Timing Reference Code)

	Bit 7	Bit 6	Bit5 (V)	Bit4 (H)	Bit3 (P3)	Bit2 (P2)	Bit1 (P1)	Bit0 (P0)
SAV during active video	1	0	0	0	0	0	0	0
EAV during active video	1	0	0	1	1	1	0	1
SAV during vertical blanking	1	0	1	0	1	0	1	1
EAV during vertical blanking	1	0	1	1	0	1	1	0

Table 3-9 The Value of Fourth Byte In Every Case (Even Field Timing Reference Code)

	Bit 7	Bit 6	Bit5 (V)	Bit4 (H)	Bit3 (P3)	Bit2 (P2)	Bit1 (P1)	Bit0 (P0)
SAV during active video	1	1	0	0	0	1	1	1
EAV during active video	1	1	0	1	1	0	1	0
SAV during vertical blanking	1	1	1	0	1	1	0	0
EAV during vertical blanking	1	1	1	1	0	0	0	1

3.14.2 Typical Application

The still image or video captured by the external image sensor is first sent to camera interface for line transformation, scaling and data format conversion, and then stored temporarily in external RAM. If end users want to preview the image/video instantly, the image/video stored in RAM is sent to LCD controller without any further processing. If end users would like to save the image/video, the data is sent to image/video processor for compression, and sent back to RAM after compression.

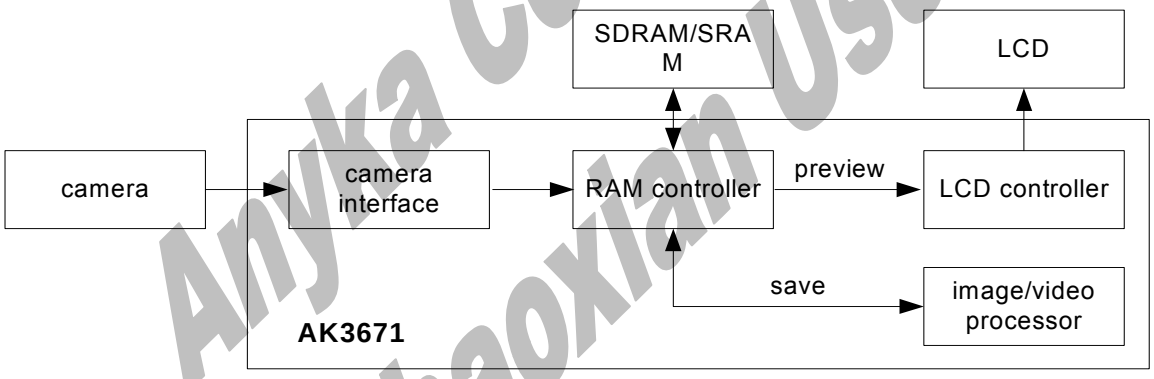


Figure 3-23 Typical Application of Camera Interface

3.15 LCD Controller

The basic function of the LCD controller is to refresh the LCD display from the display memory at each CPU command. The LCD controller of AK3671 processor supports black-

and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels with programmable resolutions and video timings.

The LCD controller supports:

- 8-bit (4K/64K color) / 9-bit (9-bit x 2 transfers, 256K color)/16-bit (4K/64K color) MPU interface
- maximum QVGA resolution
- reading back function when connecting to a MPU LCD panel
- down scaling function when the input format is YCbCr 4:2:2
- YCbCr 4:2:2, RGB5:6:5 and BGR5:6:5 input format
- RGB output format
- user programmable video timing
- user programmable video resolutions
- 16-bit DMA interface
- operating from a wide range of frame fresh rates
- static synchronization
- full synthesizability

Table 3-10 Supported Input/Output Image/Video Resolutions

FORMAT				RGB/BGR	YCbCr
INPUT	MIN	HORIZONTAL		18	18
		VERTICAL		17	17
	MAX	HORIZONTAL		1022	1022
		VERTICAL		1023	1023
OUTPUT	MIN	HORIZONTAL		17	-
		VERTICAL		17	-
	MAX	NO SCALING	HORIZONTAL	1022	-
			VERTICAL	1023	-
		DOWN SCALED	HORIZONTAL	320	-
			VERTICAL	1023	-

3.15.1 Working Modes

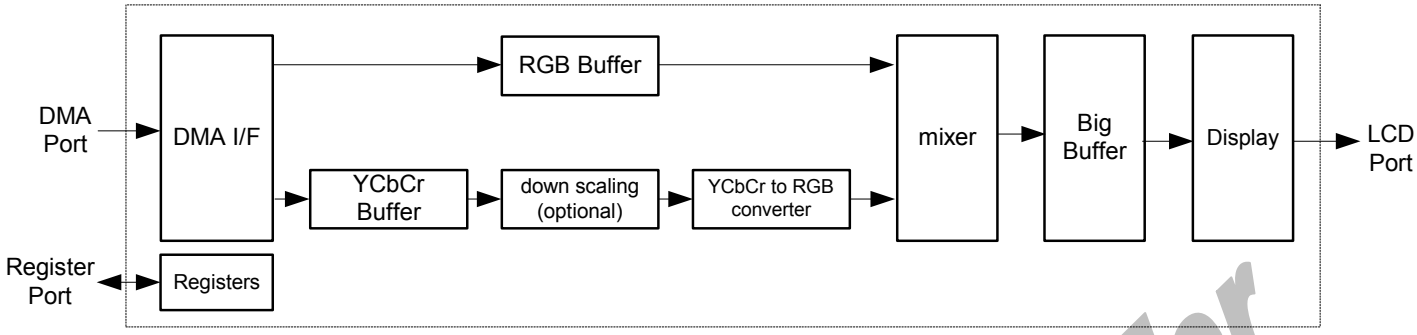


Figure 3-24 LCD Controller Internal Architecture

At the command of CPU, LCD controller can work under 2 active modes:

1) DMA-Based Mode

a) Only one picture is input from DMA port

- Input data format is YCbCr 4: 2:2 format

LCD controller accepts data from DMA port, stores the data in YCbCr buffer, and scales the image to desired size, if necessary. Then it converts YCbCr format to RGB format, stores the image in big buffer temporarily, and finally sends to LCD port for display.

The image DOWN scaler may be turned on to change the horizontal and vertical sizes of the image from DMA port. The scaler is possible to provide arbitrary scaling ratio of M/N where the values of M and N range from 16 to 1024 (M>=N).

The embedded YCbCr to RGB converter module translates the YCbCr data to RGB data using combinational logic. The actual coefficients used in the hardware implementation are:

R = Y + 1.4022× (Cb-128)

G = Y- 0.7145×(Cb-128) - 0.3456×(Cr-128)

B = Y+1.7710×(Cr-128)

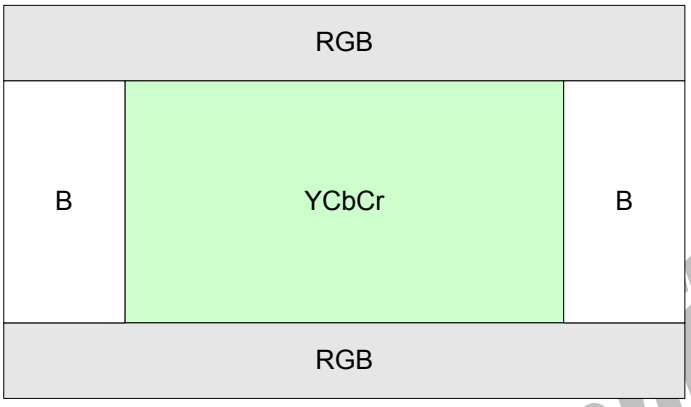
- Input data format is RGB5:6:5/BGR5:6:5 format

LCD controller accepts data from DMA port, stores the data in big buffer, and sends to LCD port for display.

b) Two pictures are input from DMA port concurrently

The LCD controller supports two pictures input from DMA port concurrently: the foreground picture should be in YCbCr format; while the background picture, in RGB format. The two pictures are sent to the YCbCr buffer and RGB buffer respectively. The picture of YCbCr can be down scalded and converted to RGB format. Then the foreground picture and background picture are sent to the mixer. Finally, the mixed data is sent to the big buffer and LCD panel in succession.

One thing should be paid special attention to, that is, when displayed on a RGB LCD panel, the two pictures have the relationship as shown in Figure 3-25.



ITEM	INPUT FORMAT	BUFFER	OUTPUT FORMAT
Picture 1	RGB5:6:5/ BGR5:6:5	RGB Buffer	RGB
Picture 2	YCbCr4:2:2	YCbCr Buffer	RGB

Figure 3-25 Relationship of Two Pictures

Note: The areas of "B" displayed a single color (defined by software engineers) rather than the background picture.

2) CPU Mode

The data is written into a specific register, and then sent to LCD port without any processing through register bus.

3.15.2 Timing and Data format

3.15.2.1 MPU Interface

3.15.2.1.1 16-bit MPU Interface

1. Timing Diagrams

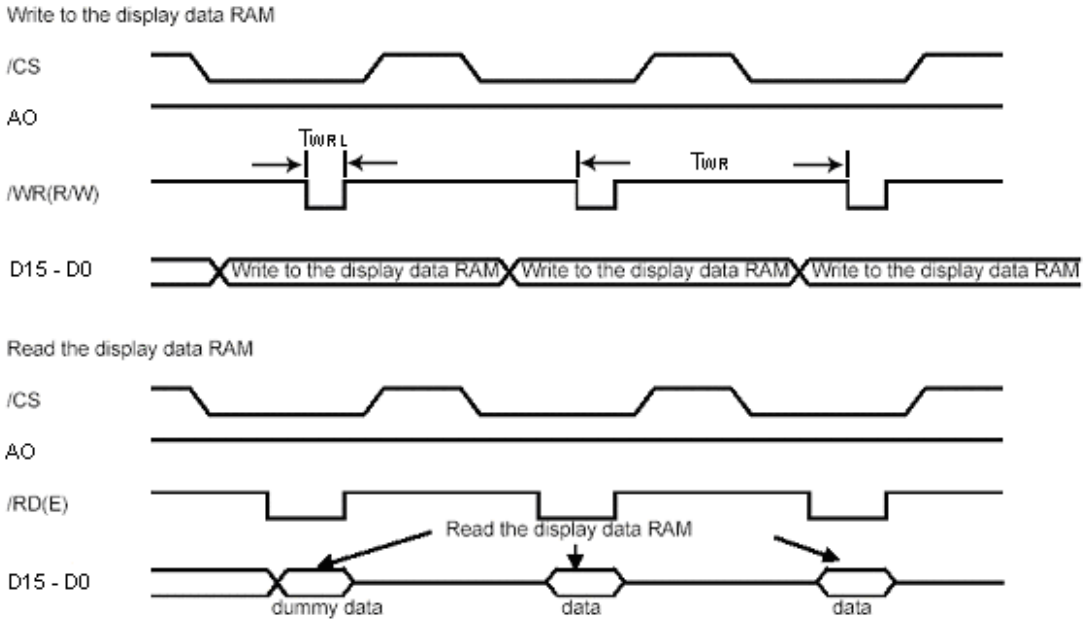


Figure 3-26 16-bit Timing Diagram 1 (DMA-based Mode)

Note: T_{WRL} and T_{WR} are configurable by corresponding registers.

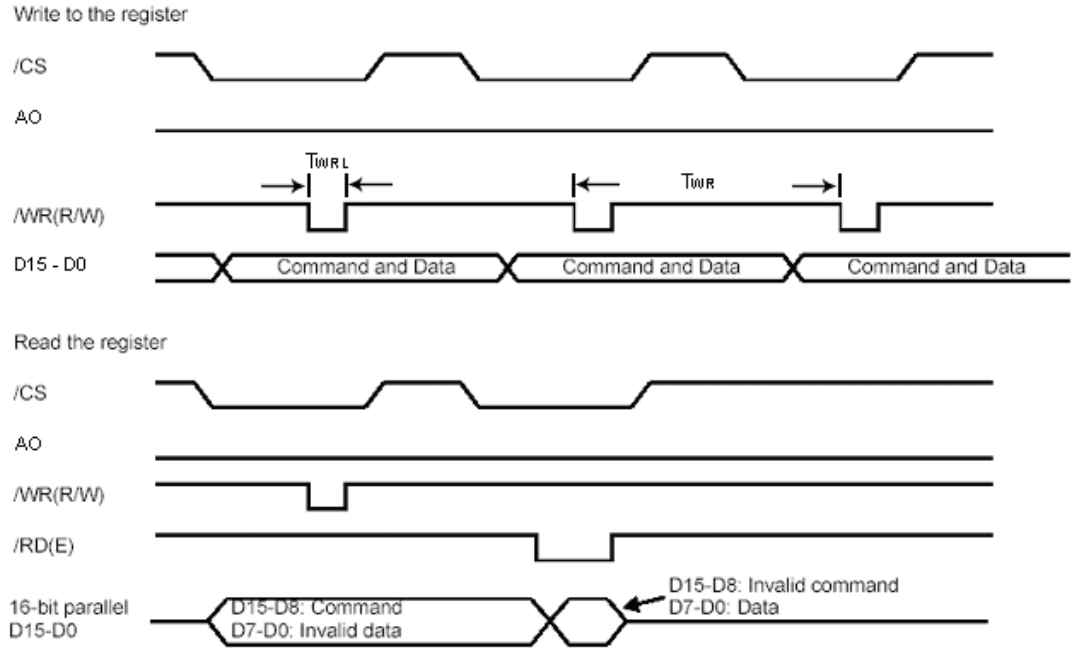
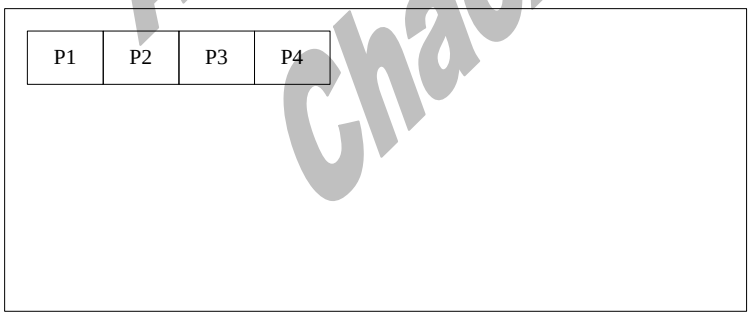


Figure 3-27 16-bit Timing Diagram 2 (CPU Mode)

Note: T_{WRL} and T_{WR} are configurable by corresponding registers.

2. Memory Data Format

MEMORY ADDRESS	D[7:0]	DUMMY DATA	Pixel
0x00	R7 – R3 (D[7:3]) or B7 – B3 (D[7:3])	D[2:0]	P1
0x01	G7 - G2(D[7:2]) or G7 - G2(D[7:2])	D[1:0]	P1
0x02	B7 – B3(D[7:3]) or R7 – R3(D[7:3])	D[2:0]	P1
0x03	R7 – R3(D[7:3]) or B7 – B3(D[7:3])	D[2:0]	P2
0x04	G7 - G2(D[7:2]) or G7 - G2(D[7:2])	D[1:0]	P2
0x05	B7 – B3(D[7:3]) or R7 – R3(D[7:3])	D[2:0]	P2
...	...		...



3. data pins

PIN	MPU_ AD[15]	MPU_ AD[14]	MPU_ AD[13]	MPU_ AD[12]	MPU_ AD[11]	MPU_ AD[10]	MPU_ AD[9]	MPU_ AD[8]
POWER	D15 (MSB)	D14	D13	D12	D11	D10	D9	D8
COLOR	R7	R6	R5	R4	R3	G7	G6	G5

PIN	MPU_ AD[7]	MPU_ AD[6]	MPU_ AD[5]	MPU_ AD[4]	MPU_ AD[3]	MPU_ AD[2]	MPU_ AD[1]	MPU_ AD[0]
POWER	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
COLOR	G4	G3	G2	B7	B6	B5	B4	B3

3.15.2.1.2 9-Bit/8-bit MPU Interface

1. Timing Diagrams

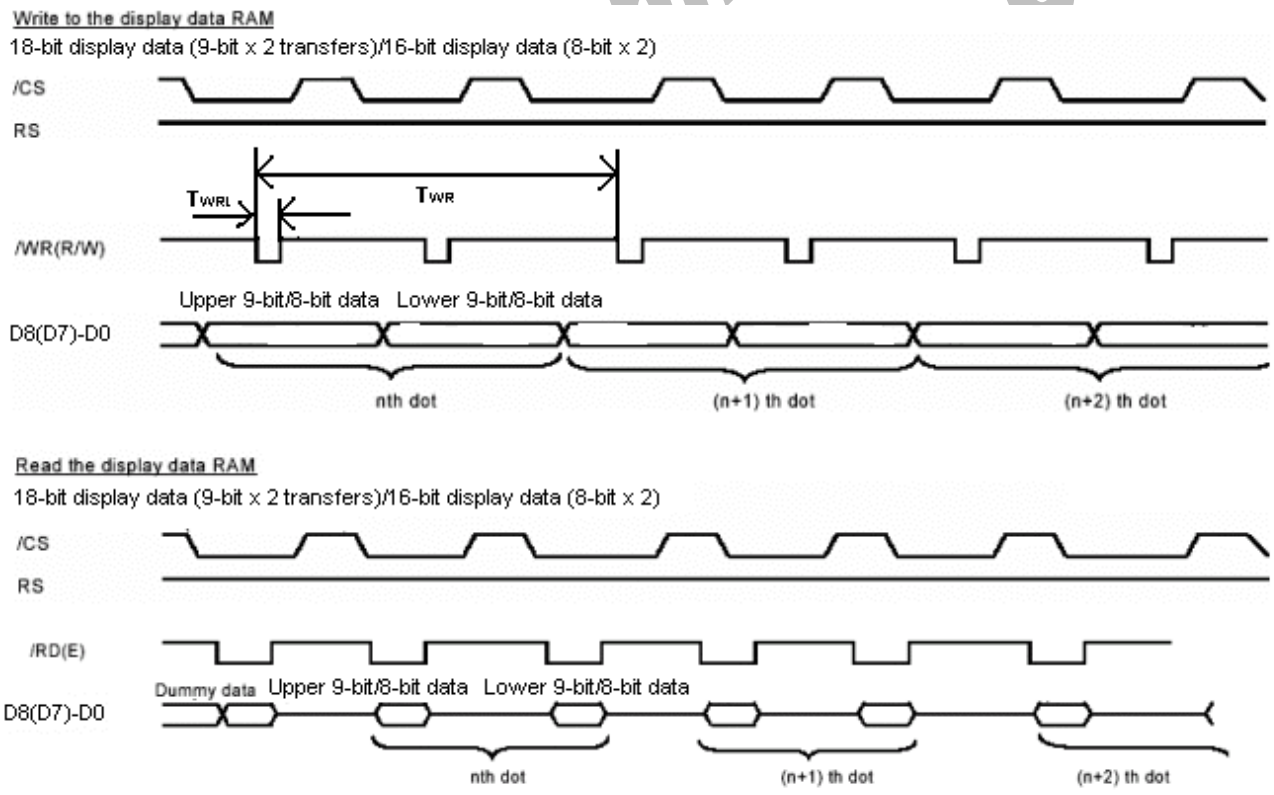


Figure 3-28 MPU 9-bit/8-bit Mode Timing Diagram

Note: T_{WRL} and T_{WR} are configurable by corresponding registers.

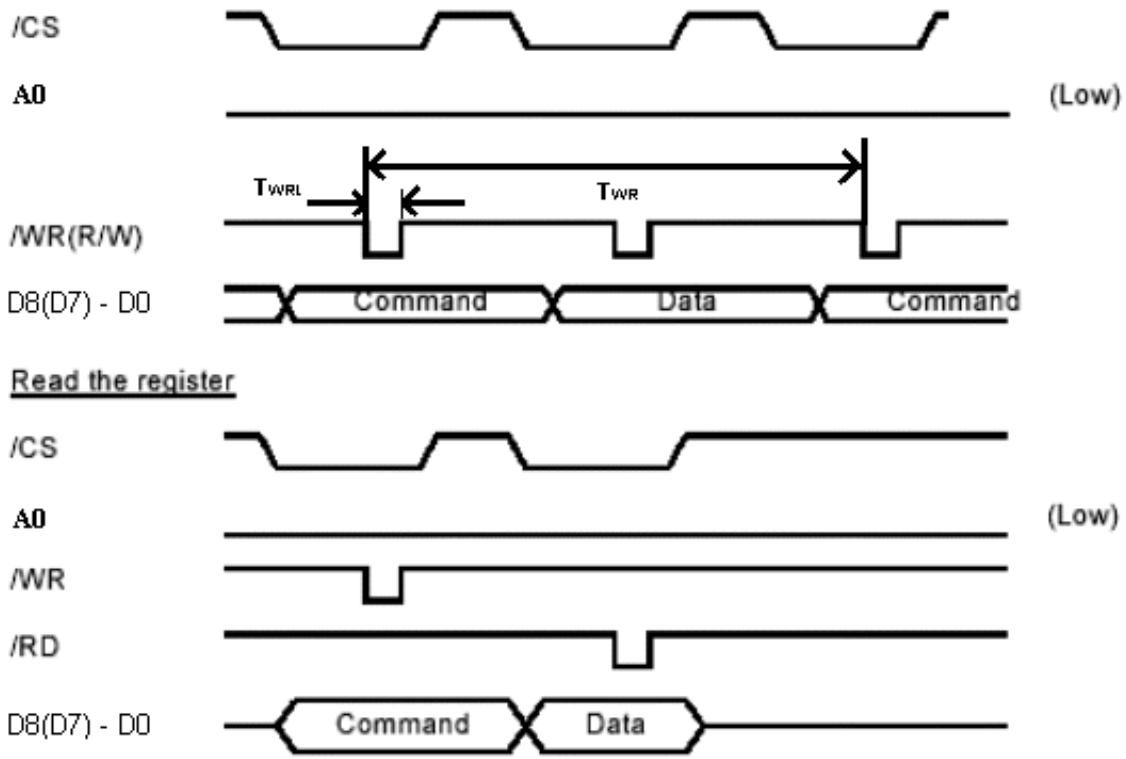
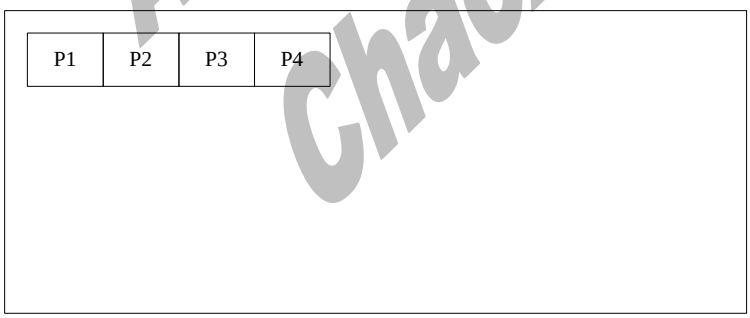


Figure 3-29 MPU 9-bit/8-bit Mode Timing Diagram

Note: T_{WRL} and T_{WR} are configurable by corresponding registers.

2. Memory Data Format

MEMORY ADDRESS	9 bits		8 bits		Pixel
	D[7:0]	DUMMY DATA	D[7:0]	DUMMY DATA	
0x00	R7 - R2 (D[7:2]) or B7 - B2 (D[7:2])	D[1:0]	R7 – R3 (D[7:3]) or B7 – B3 (D[7:3])	D[2:0]	P1
0x01	G7 - G2(D[7:2]) or G7 - G2(D[7:2])	D[1:0]	G7 - G2(D[7:2]) or G7 - G2(D[7:2])	D[1:0]	P1
0x02	B7 - B2 (D[7:2]) or R7 - R2 (D[7:2])	D[1:0]	B7 – B3(D[7:3]) or R7 – R3(D[7:3])	D[2:0]	P1
0x03	R7 - R2 (D[7:2]) or B7 - B2 (D[7:2])	D[1:0]	R7 – R3(D[7:3]) or B7 – B3(D[7:3])	D[2:0]	P2
0x04	G7 - G2 (D[7:2]) or G7 - G2 (D[7:2])	D[1:0]	G7 - G2(D[7:2]) or G7 - G2(D[7:2])	D[1:0]	P2
0x05	B7 - B2 (D[7:2]) or R7 - R2 (D[7:2])	D[1:0]	B7 – B3(D[7:3]) or R7 – R3(D[7:3])	D[2:0]	P2
...	...	...	...		...



3. Data Pins

- 9-bit MPU Interface

PIN	MPU_ AD[8]	MPU_ AD[7]	MPU_ AD[6]	MPU_ AD[5]	MPU_ AD[4]	MPU_ AD[3]	MPU_ AD[2]	MPU_ AD[1]	MPU_ AD[0]	
POWER	D8 (MSB)	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	1st transfer
COLOR	R7	R6	R5	R4	R3	R2	G7	G6	G5	
POWER	D8 (MSB)	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	2nd transfer
COLOR	G4	G3	G2	B7	B6	B5	B4	B3	B2	

- 8-bit MPU Interface

PIN	MPU_ AD[7]	MPU_ AD[6]	MPU_ AD[5]	MPU_ AD[4]	MPU_ AD[3]	MPU_ AD[2]	MPU_ AD[1]	MPU_ AD[0]	
POWER	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	1st transfer
COLOR	R7	R6	R5	R4	R3	G7	G6	G5	
POWER	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	2nd transfer
COLOR	G4	G3	G2	B7	B6	B5	B4	B3	

3.15.3 Black-and-White Panels and Gray-Scale Panels

If black-and-white panels/gray-scale panels are employed, CPU mode is recommended. Because the black-and-white panels are always defined by 1 bit of display data for each pixel, and the commonly seen gray-scale panels are defined by 16 gray levels, which use 2 bits or 4 bits of display data for each pixel.

3.16 UART

The UART port provides serial communication capability with external devices through an RS232 cable. Serving as DTE, the UART can operate in polling-based mode, interrupt-based mode, DMA-based mode and CPU mode.

The UART transmits/receives a data packet of 10 bits: 1 start bit (always “0”), 8 data bits, and 1 stop bit (should be “1”)(no parity bit). To transmit, data is written from the peripheral data bus to the 64-byte transmit FIFO. This data is passed serially out on the transmit pin (UTD). To receive, data is received serially from the receive pin (URD) and stored in the 64-byte receive FIFO.

The UART generates baud rates based on the input clock (ASIC CLK) and a configurable divider. The relationship among baud rate, ASIC CLK and divider is: $baudrate = \frac{ASICCLK}{16 \times divider}$ (divider = 1, 2, …2 ^{16}).

Note: There is no default value of the baud rate for UART. Programmers should set it first before data communication.

3.17 SPI

The SPI interface, which can be programmed to work in either master mode or slave mode, allows fast synchronous serial communication of 8-bit data length. When the SPI interface is used as master, transmission frequency is configurable by setting the clock divider ratio, and a byte transmit/receive operation starts with host writing data into the transmit FIFO. When the SPI interface is used as slave, external bus master supplies the clock. Equipped with a 64-byte transmit FIFO and a 64-byte receive FIFO, the SPI interface also supports DMA-based mode and CPU mode.

Notes:

1. When the SPI interface works in master mode, AK3671 has to continuously send data to supply the clock.
2. When the SPI interface works in slave mode, AK3671 should provide an instruction set for master’s accessing. It fills “0”s in the transmit FIFO if the transmit FIFO is empty.

Table 3-7 lists the pins of SPI interface, all of which are shared with those of other functional blocks.

Table 3-11 Pin Definitions of SPI Interface

PIN	TYPE	PULLUP/ PULLDOWN	DESCRIPTION	SHARED WITH
#SPI_CS	I/O	PPU	SPI chip select, active low.	GPIO[6]
SPI_CLK	I/O	PPD	SPI clock.	NFC_ALE/ MPU_AD[9]
SPI_MOSI	I/O	PPD	In host mode, data output; in client mode, data input.	NFC_CLE/ MPU_AD[8]
SPI_MISO	I/O	PPU	In host mode, data input; in client mode, data output.	#NFC_WR/ MPU_AD[10]

Note: PPU: Programmable Pullup (The word “programmable” means that the pull-up function attached to the corresponding ports is configurable (enabled or disabled) by corresponding registers. Default status is that the pull-up/pull-down function attached to the corresponding port is enabled.)

The SPI can be programmed to work in any of the following four timing waveforms.

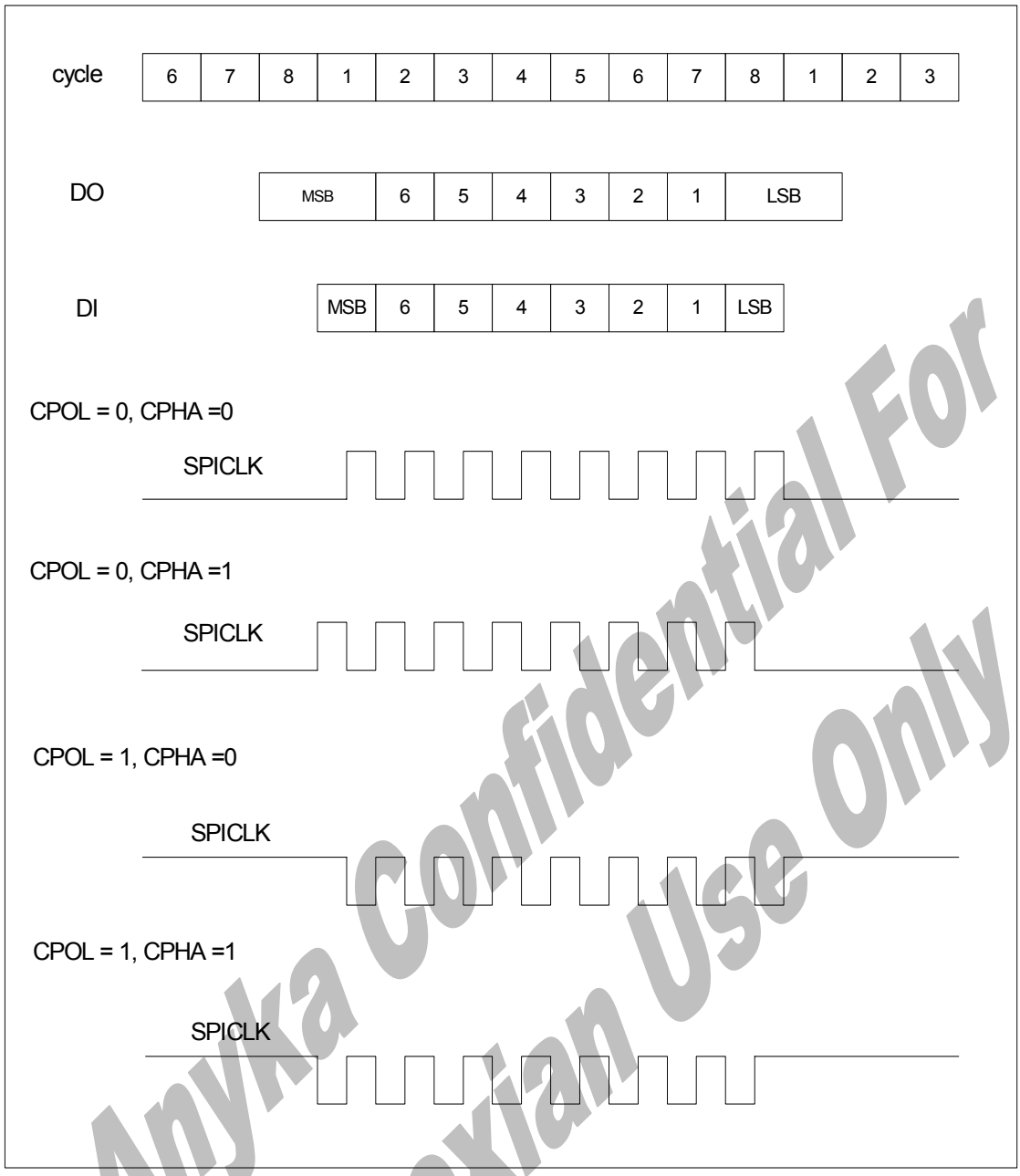


Figure 3-30 SPI Timing Diagram

3.18 USB 2.0 HS Device

The USB 2.0 HS device, fully compliant with USB Specification Version 2.0 (HS), operates as a function controller for a high-speed/full-speed USB peripheral.

The USB controller provides all the encoding, decoding and checking needed in sending and receiving USB packets. That is, the USB controller interrupts the CPU only when endpoint data has been successfully transferred.

In addition to endpoint 0, the USB 2.0 HS Device provides 3 endpoints that can be configured to be used as transmit endpoints or receive endpoints. FIFOs are shared by a transmit endpoint and the correspondingly numbered receive endpoint. The function and FIFO size of each endpoint are as follows:

ENDPOINT	FUNCTION(usually)	FIFO SIZE
Endpoint 0	Control endpoint	64 Bytes
Endpoint 1	Interrupt endpoint	64 Bytes
Endpoint 2	Bulk endpoint	1024 Bytes
Endpoint 3	Bulk endpoint	1024 Bytes

3.19 MMC/SD Interface

The Multimedia Card (MMC) is a universal low cost data storage and communication medium implemented as a hardware card with a simple control unit and a compact, easy-to-implement interface. MMC communication is based on an advanced 7-pin serial bus designed to operate in a low voltage range at medium speed.

The Secure Digital Card (SD) is an evolution of the MMC with an additional 2 PINs in the form factor that is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in new audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are compatible with the MMC. The SD is composed of a memory card and an I/O card. The memory card includes a copyright protection mechanism that complies with the security requirements of the Secure Digital Music Initiative (SDMI) standard, and is faster and has a higher memory capacity. The I/O card combines high-speed data I/O with low-power consumption for mobile electronic devices.

The features of MMC/SD interface are as follows:

- conforming to *The Multimedia Card Specification, Version 4.0* and *SD Memory Card Specification, Version 2.0*

- supporting one-bit, four-bit, and eight-bit data bus
- maximum reading/writing speed is half of ASIC CLK
- 32-bit local buffer
- working in DMA mode or CPU mode
- working in little endian only
- supporting single block operation， multiple block operation and stream mode (MMC card only)

Note: As defined in the *The Multimedia Card Specification*, the data will not be followed by the CRC bits when it is transferred in stream mode.

MMC/SD interface contains 10 pins.

Table 3-12 MMC/SD Interface PIN Definitions

PIN	TYPE	PULLUP/ PULLDOWN	DESCRIPTION	SHARED WITH	RESET STATE
MCK	O	-	MMC/SD operating clock.	GPIO[31]	GPIO[31]
MCMD	I/O	-	MMC/SD command.	#NFC_RD	#NFC_RD
MMC_data[7:0]	I/O	PPU	MMC/SD data bus.	NFC_data[7:0]/ MPU_AD[7:0]	NFC_data[7:0]

Note: PPU: Programmable Pullup (The word “programmable” means that the pull-up function attached to the corresponding ports is configurable (enabled or disabled) by corresponding registers. Default status is that the pull-up/pull-down function attached to the corresponding port is enabled.)

Communication over the MMC/SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit. The MMC/SD controller first sends the command to the card and waits response before data transmitting.

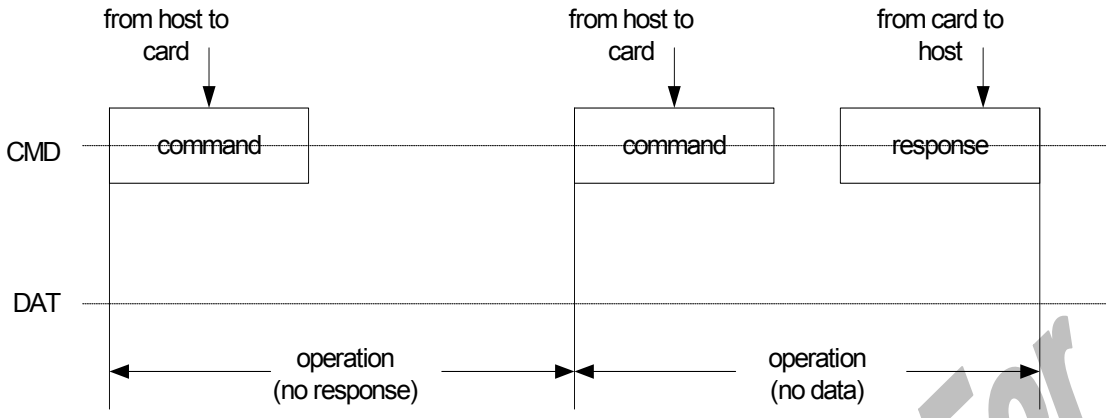


Figure 3-31 “No Response” and “No Data” Operations

Data transmission to/from the MMC/SD card are done in blocks, which are always followed by CRC bits. There are two kinds of block operations: Single Block Operation and Multiple Block Operations. (The Multiple block operation mode is better for fast write operation.) A multiple block transmission is terminated when a stop command follows on the CMD line.

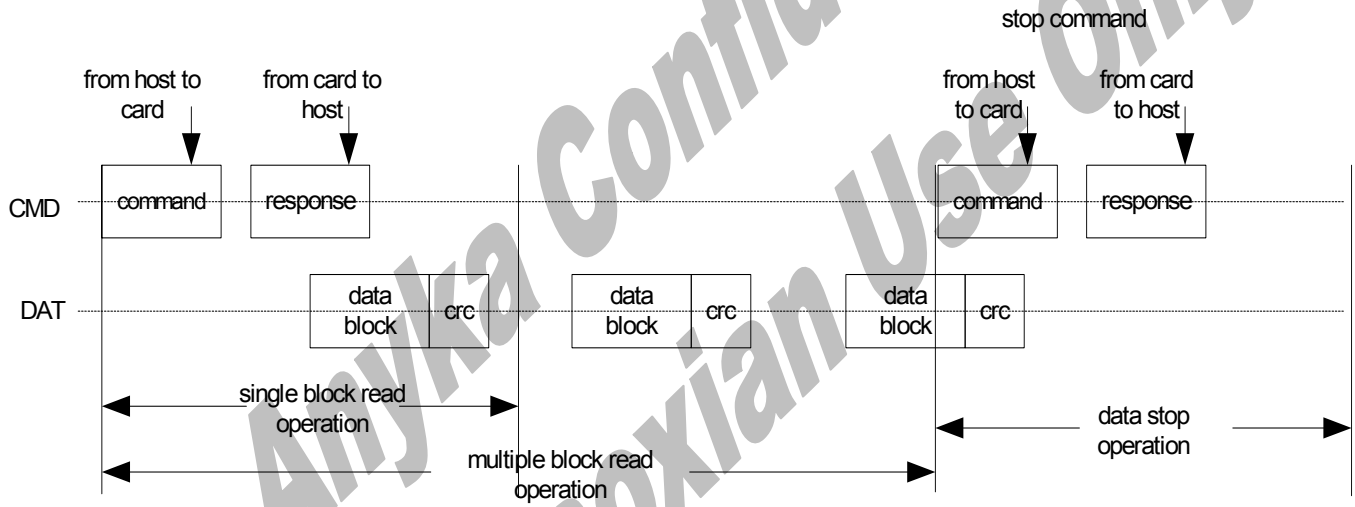


Figure 3-32 Single and Multiple Block Read Operation

The block write operation uses a simple busy signal on the DAT0 data line regardless of the number of data lines used for transferring the data.

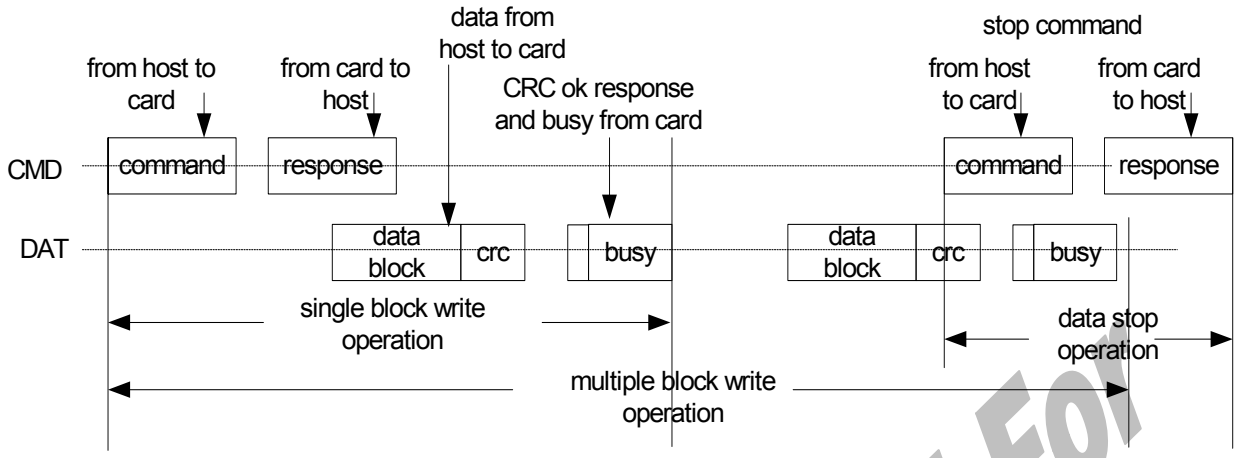


Figure 3-33 Single and Multiple Block Write Operation

Command tokens have the following coding schehme:

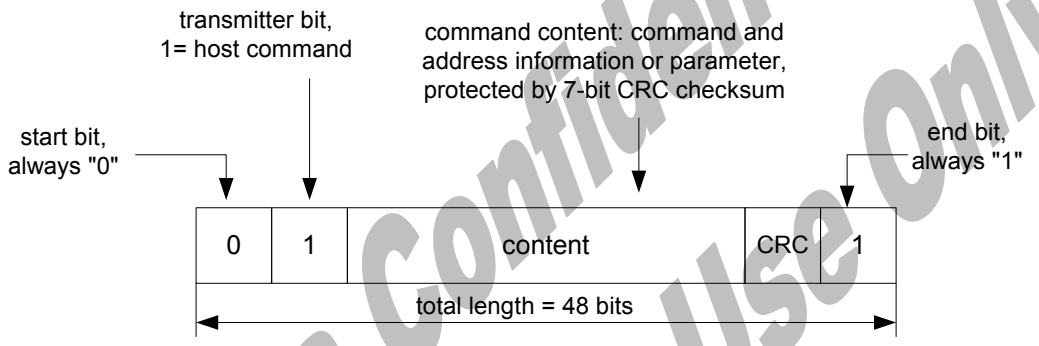


Figure 3-34 Command Token Format

Each command token is preceded by a start bit (“0”) and succeeded by an end bit (“1”). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated.

Response tokens have four coding schemes depending on their content. The token length is either 48 bits or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

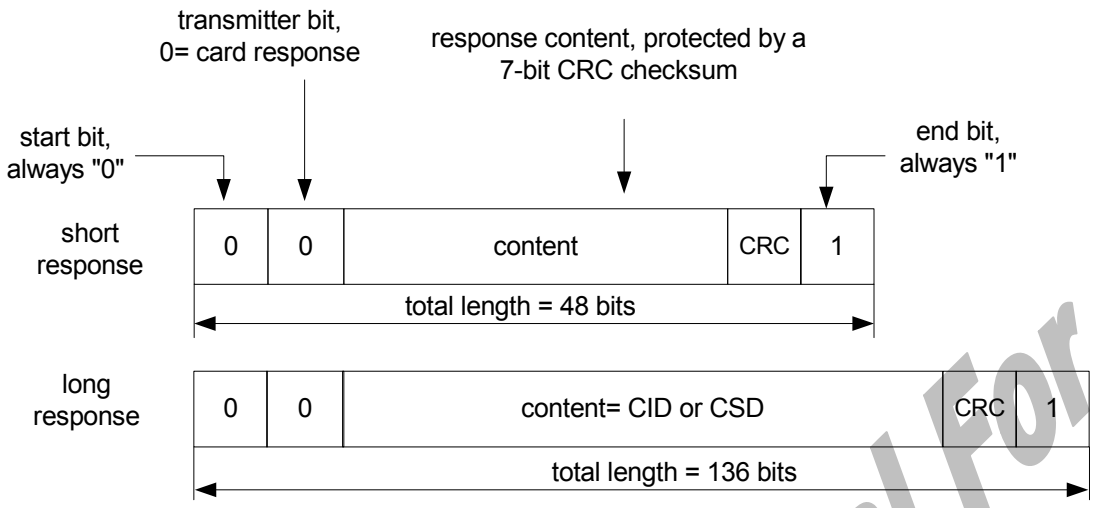


Figure 3-35 Response Token Format

In the CMD line the MSB is transmitted first and the LSB is the last.

When the 4-bit/8-bit option is used, the data is transferred 4 bits/8 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for every data line. And CRC bits are calculated and checked for every data line respectively. The CRC status response and Busy indication will be sent by the card to the host on data[0] only. (Data[1], data[2], …, data[7] don't care during that period.)

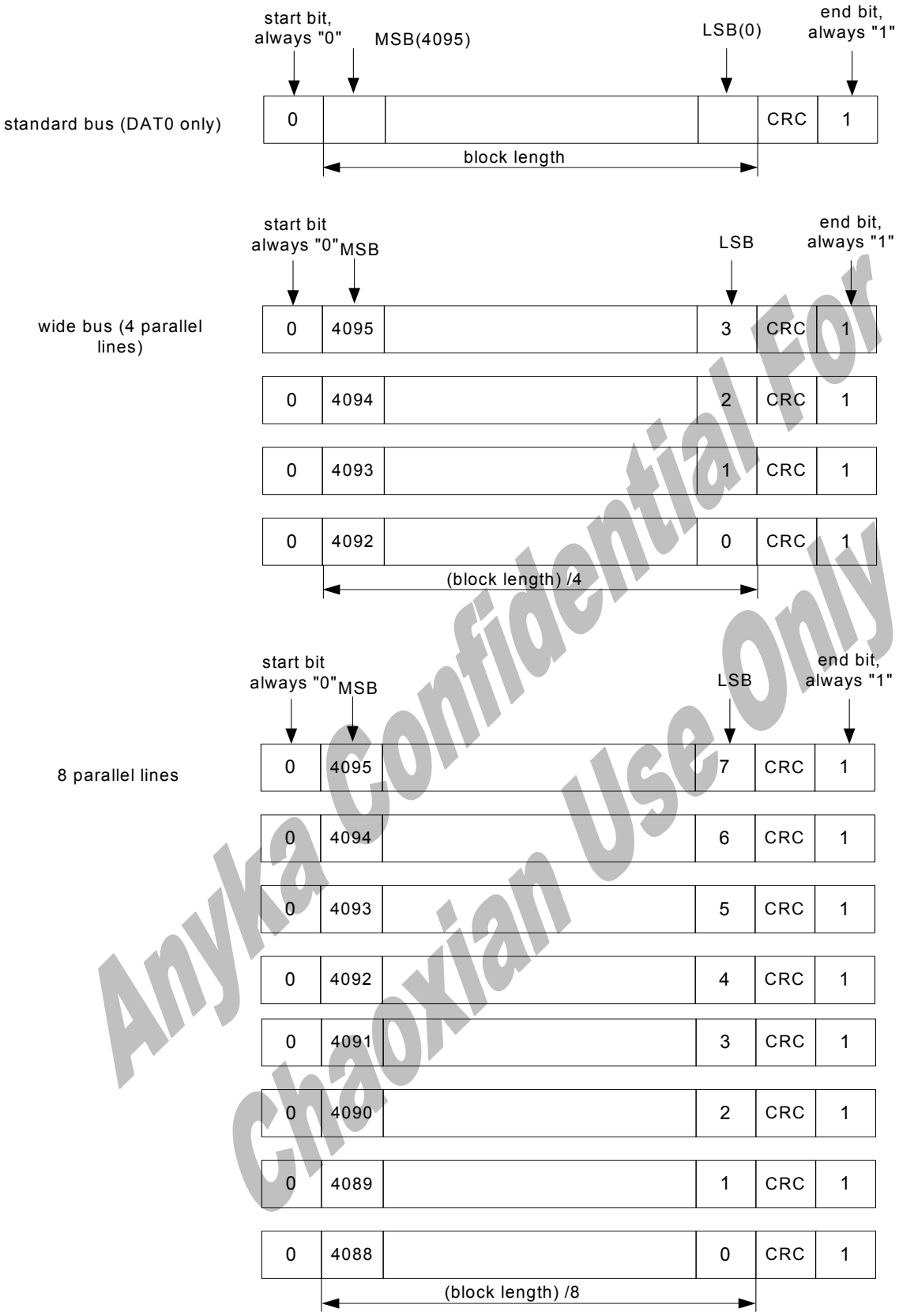


Figure 3-36 Data Packet Format

3.20 Audio Analog Components

The audio analog components consist of

- one 16-bit sigma-delta ADC
- one 10-bit SAR ADC
- two 18-bit sigma-delta DACs
- class AB power amplifier
- headphone driver
- microphone interface
- line in interface
- touch screen interface
- battery monitor
- temperature detector
- one reference voltage generator

To make architecture presentation easier, the digital filters associated with the sigma-delta D/A converters are included.

3.20.1 ADCs

As shown in Figure 3-37, AK3671 contains one 10-bit SAR ADC (ADC1) and one 16-bit sigma-delta ADC (ADC2). ADC1 includes six channels, four for touch panel and one for battery measurement and one general-purpose AD input channel. ADC2 accepts data from microphone interface or line in interface. The input voltage of ADC1 ranges from 0.1V to 3.2V and the maximum driven current for touch screen is 100mA. While the full scale input of ADC2 is from 0.1V to 2.8V at AVDD = 3.3V.The sampling rate of both ADC1 and ADC 2 is 48KBPS.

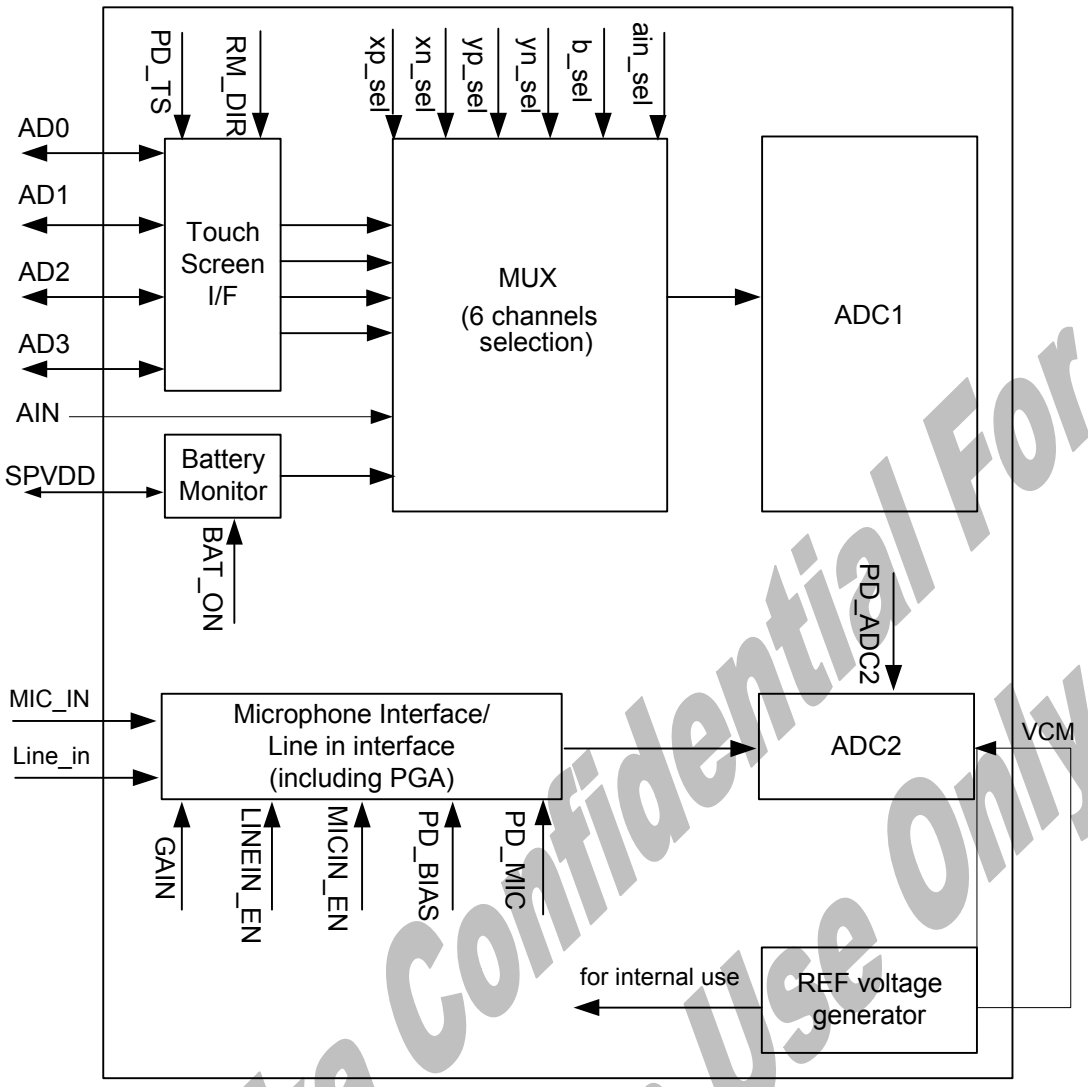


Figure 3-37 Architecture of Embedded ADCs

Notes:

1. *AD0, AD1, AD2, AD3, SPVDD, MIC_IN, Line_in*, *VCM* and *AIN* are external pins. Please refer to Chapter 2 for details.

2. PD_TS: power down touch screen interface; RM_DIR: remove touch screen driver; xp_sel: select X positive; xn_sel: select X negative; yp_sel: select Y positive; yn_sel: select Y negative; b_sel: select battery monitor input (SPVDD); ain_sel: select the general-purpose AD input; BAT_ON: enable battery monitor.

3. GAIN: PGA control; LINEIN_EN: enable line in; MICIN_EN: enable microphone; PD_BIAS: power down bias reference voltage; PD_MIC: power down microphone interface; PD_SDM: power down ADC2.

4. The touch screen driver contained in the touch screen interface can be disabled by software. That is, under software control, AD0, AD1, AD2 and AD3 can be used as general purpose ADC input channels.

3.20.1.1 Reference Voltage Generator

The reference generator generates a reference voltage for analog module internal use and a voltage for ADC2.

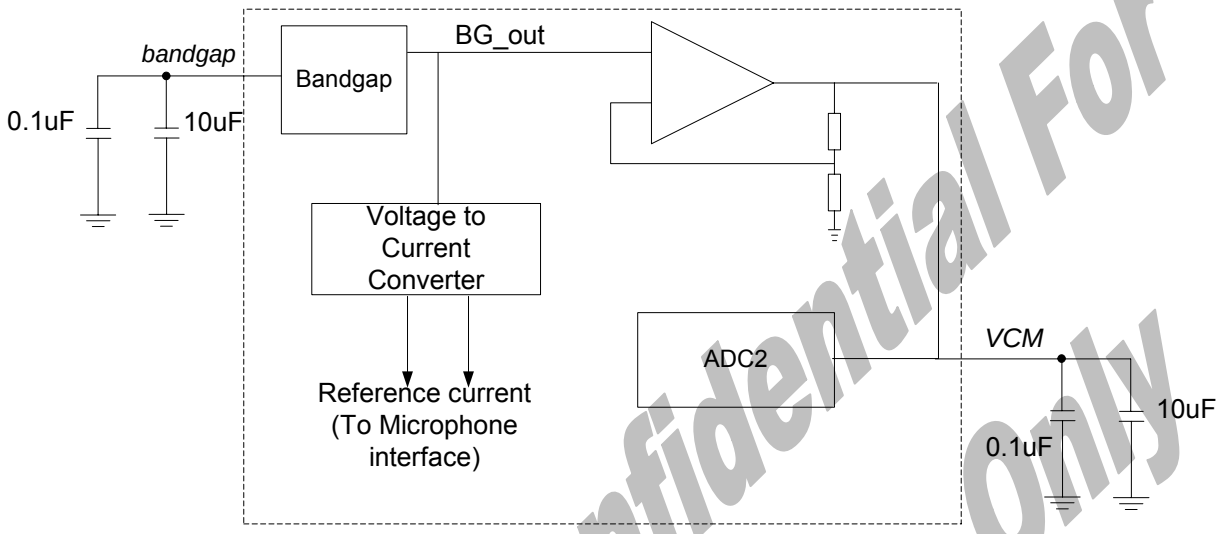


Figure 3-38 Reference Voltage Generator

Note: *VCM* and *bandgap* are external pins. Please see details in chapter 2.

3.20.1.2 Touch Screen Interface

The touch screen interface supports 4-wire resistive touch screens, which work by applying a voltage across the vertical or horizontal resistive network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input stylus, pen or finger. The change in the resistance ratio marks the location on the touch screen. The ADC converts the voltage measured at the point the panel is touched. A measurement of the Y position is made by connecting the XP input to ADC, turning on the YP and YN drivers, and digitalizing the voltage seen at the XP input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the XP lead doesn't affect the conversion due to the high input impedance of the ADC. Voltage is then applied to the other axis, and the ADC converts the voltage representing the X position on the screen through the YP input. This provides the X and Y coordinates to the associated processor. The time from the first sample period to analog-to-digital's

converting, and from XP/YP connecting to a voltage to disconnecting can be configured by software.

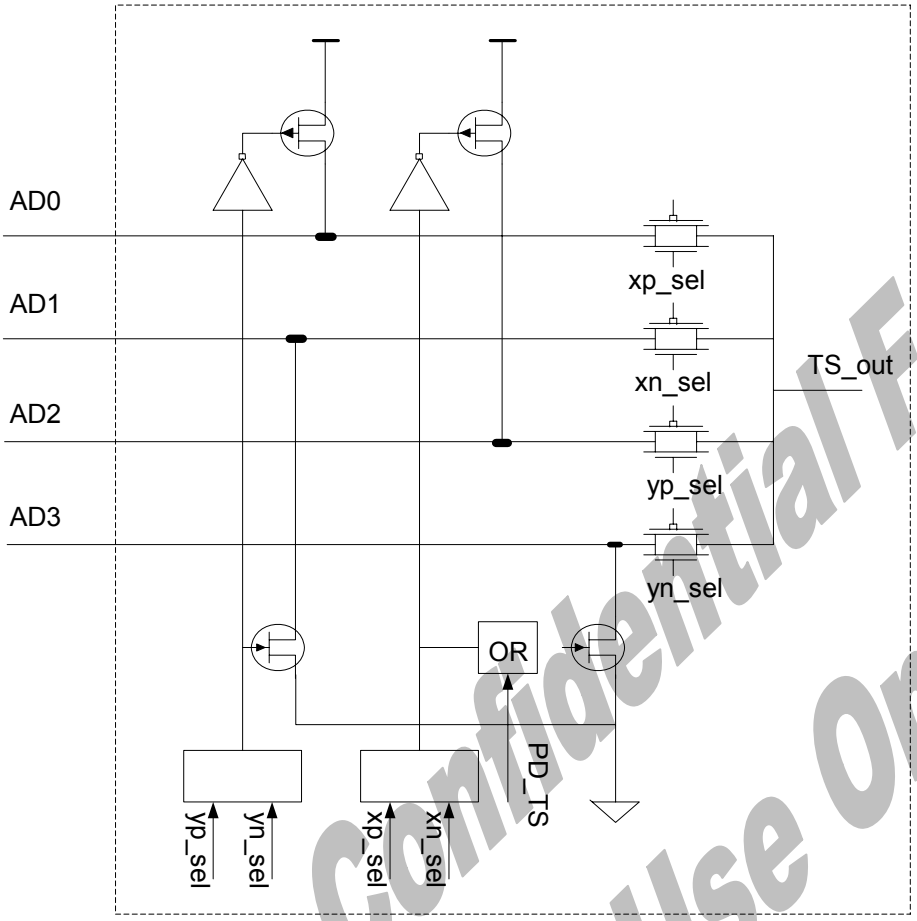


Figure 3-39 Touch Screen Interface

3.20.1.3 Battery Monitor

The battery monitor measured the data input from the external pin SPVDD.

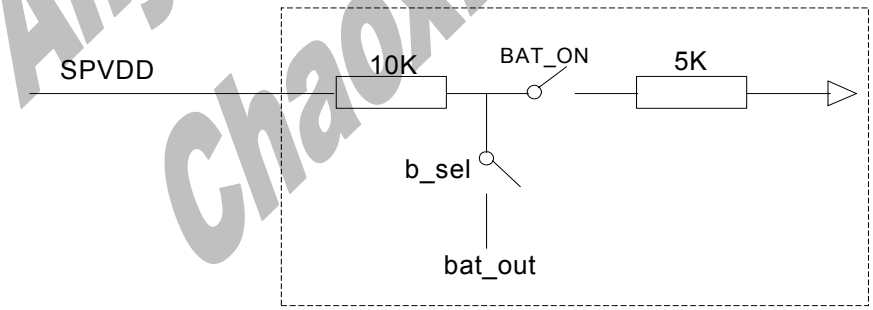


Figure 3-40 Battery Monitor

3.20.1.4 Microphone Interface

The high impedance and low capacitance microphone interface can be connected to a wide range of monophonic microphones of different dynamics and sensitivities. It contains a programmable gain amplifier (PGA), a reference voltage generator and a current generator.

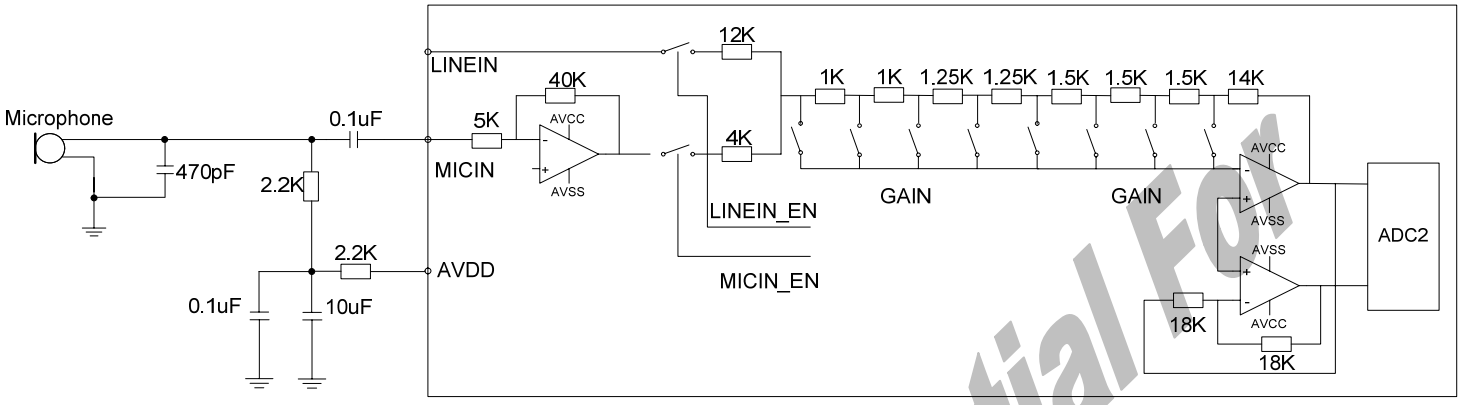


Figure 3-41 Microphone Interface Architecture

Notes:

1. *LINE IN, MICIN* and *AVDD* are external pins.
2. The microphone interface is configurable by software to provide a gain ranging from 8 to 40 times. To maximize the SNR, the gain should be configured to meet the requirement that the maximum signal ADC receives is within its full scale (from 0.65V to 2.65V (p-p) at AVDD = 3.3V).
3. This circuit is applicable to the condenser microphones.
4. The external bias circuit of microphone above is for reference only. It is subject to the changing microphones.

3.20.2 DACs

One of AK3671's remarkable features is that it embeds headphone driver and class AB power amplifier, both of which accept input from either DACs or LINE IN. The the maximum input bit rate of the DACs is 180KB/s.

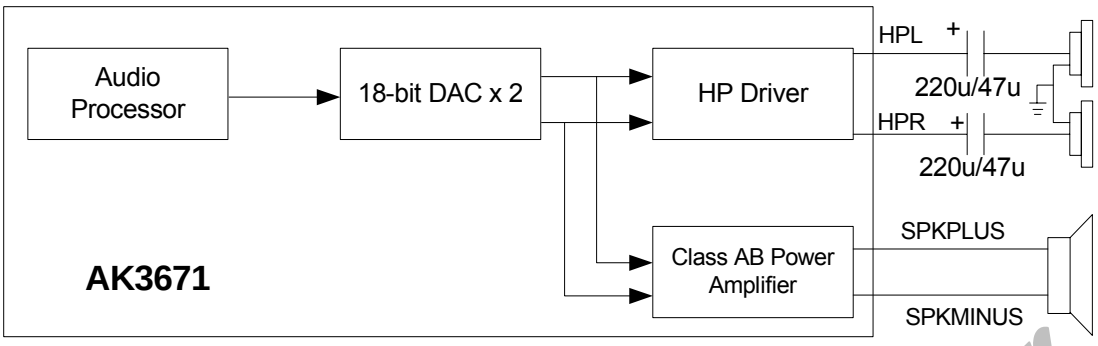


Figure 3-42 Audio Source From DACs

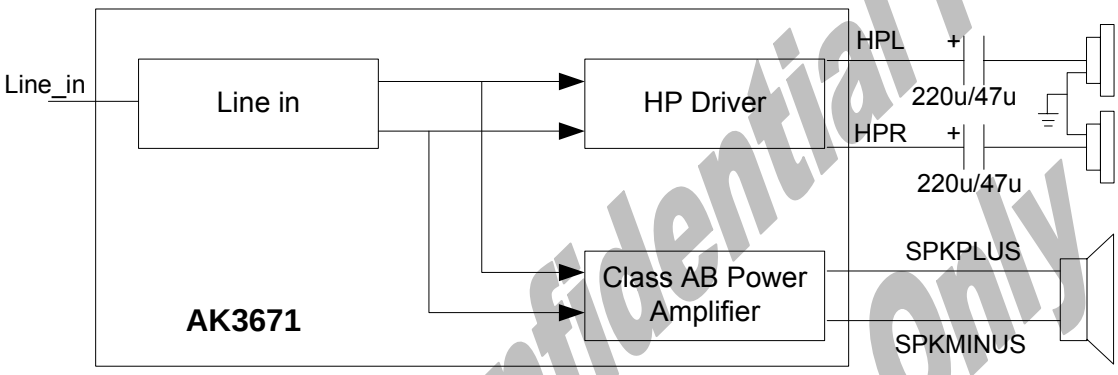


Figure 3-43 Audio Source From LINE IN

The headphone driver, which may provide a 0db, 2db, 4db or 6db gain by software configuration, is able to drive the ac-coupled resistive load up to 32ohm. And the class AB power amplifier outputs as high as 620mW at 8 ohm and 4.2V power supply. Through software control, the external speaker may get a 0db, 2db, 4db, 6db, 8db, or 10db gain.

3.20.3 Line In Interface

The AK3671 processor supports line in recording. Input through Line in port, the data may be output directly to headphone/speaker, or be sent to the PGA and ADC2 in succession. The PGA provides a gain ranging from 0.6 times to 1.67 times.

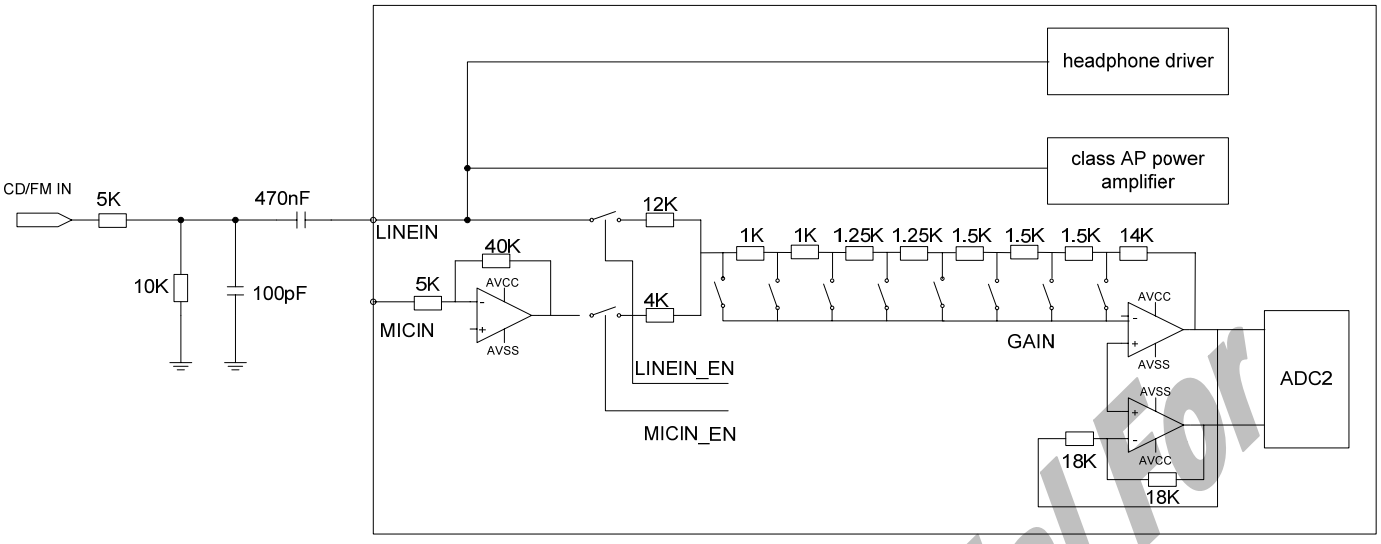


Figure 3-44 Line In Interface

3.21 PWM

The PWM controller generates an independent PWM output, which can be configured by corresponding register to control the rising-edge and falling-edge timing of a single output channel. It accepts clock signal from the pin XTAL12MI, and the supported frequency varies from 91.55Hz to 6MHz. With 16-bit high-level pulse control and 16-bit low-level pulse control, the duty cycle ranges from $\frac{1}{65536}$ (on for $\frac{1}{65536}$, and off for the other $\frac{65535}{65536}$) to $\frac{65535}{65536}$ (on for $\frac{65535}{65536}$, and off for the other $\frac{1}{65536}$).

3.22 Timers

AK3671 includes three general purpose timers and one watchdog timer. The watchdog timer protects system by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis. It sends an interrupt signal to the pin watch_dog when it reaches zero.

3.23 GPIO

Totally, AK3671 contains 31 GPIOs(namely, GPIO[31:8] and GPIO[6:0]), 3 of which are dedicated GPIOs, 28 of which are set as GPIOs by default but shared with other pins (Please see details in Section 2.2 Shared-pin List).

Apart from GPIO[14:11], all the ports are used as GPIO ports and set to input mode by default when the system is powered on. And all the ports have been attached programmable pullup/pulldown function excluding GPIO[31] and GPIO[1:0]. Additionally, with the exception of GPIO[29:28], all the other GPIO ports can work as wake-up ports to wake up the AK3671 from standby mode.

4 Electrical Specifications

4.1 Maximum Ratings

Table 4-1 AK3671 Maximum Ratings

RATING	SYMBOL	MINIMUM	MAXIMUM	UNIT
Digital Supply Voltage	VDD	-0.3	1.98	V
Digital I/O Power Voltage	VDDIO	-0.3	3.63	V
Analog Power Voltage	VDD(USB)	-0.3	3.63	V
	AVDD (ADC/DAC)	-0.3	3.63	V
	SPVDD	-0.3	4.20	V
Maximum Operating Temperature Range	T_O	-40	85	^OC
Storage Temperature	T_S	-65	150	^OC

4.2 Recommended Operating Range

Table 4-2 Recommended Operating Range

RATING	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
I/O Power Voltage	VDDIO	2.97	3.30	3.63	V
Internal Supply	VDD	1.62	1.80	1.98	V
Analog Supply Voltage	VDD (USB)	2.70	3.30	3.63	V
	AVDD (ADC/DAC)	3.13	3.30	3.47	V
	SPVDD	3.30	3.60	4.20	V
CPU Normal Operating Clock Frequency	FCPU	60	-	184	MHz
External Bus Clock Frequency	FBUS	60	-	92	MHz

4.3 DC Electrical Characteristics

Table 4-3 DC Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input High Voltage	VIH	2.0	-	VDDIO	V
Input Low Voltage	VIL	0	-	0.8	V
Output High Voltage (IOH=2.0mA)	VOH	2.4	-	-	V
Output Low Voltage	VOL	-	-	0.4	V
Input Low Leakage Current (VIN=GND, no pull-up or pull-down)	IIL	-	-	±10	uA
Input High Leakage Current (VIN=VDD，no pull-up or pull-down)	IIH	-	-	±10	uA
Output Leakage Current (VOUT=VDD, output is tri-stated	IOZ	-	-	±10	uA
Input capacitance	CI	-	-	5	pF
Output capacitance	CO	-	-	5	pF
ADC1 Full Scale (at AVDD(ADC) = 3.3V)	-	0.1	-	3.2	Vp-p
ADC2 Full Scale (at AVDD(ADC) = 3.3V)	-	0.1	-	2.8	Vp-p
Maximum Output Power (8ohm speaker at 1KHz)	Pmax	-	620	-	mW
Analog Line in Resistance	R_L	-	33K	-	ohm
Microphone Input Resistance	Rmic	-	10K	-	ohm

Notes:

1. Speaker volume control from -21db to 0 db is in 3 db steps; from 0 db to 10 db is in 2 db step.
2. Headphone volume control from -21 db to 0 db is in 3 db steps; from 0 db to 6 db is in 2 db steps.
3. All the audio parameters are measured “A weight” with a 20K LPF.

4.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 90 MHz.

Table 4-4 32K/26M Oscillator Signal Timing

PARAMETER	MIN.	TYP.	MAX.	UNIT
XTAL32K Input Jitter		5	100	ns
XTAL32K Startup Time	800			ms
XTAL12M Input Jitter		0.2		ns
XTAL12M Startup Time		600		us

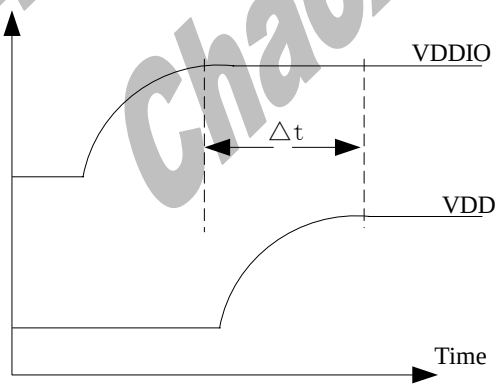
Table 4-5 CLKO Rise/Fall Time (at 10pF Loaded)

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Rise Time		2		ns
Fall Time		2		ns

Table 4-6 VDDIO and VDD Setup Time

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
VDD Setup Time			1	ms
VDDIO Setup Time			1	ms
$\triangle t$ (VDDIO to VDD)$_{Note}$			1	ms

Note:



5 PIN-Out and Package Information

AK3671 is packaged in a 144-pin QFP with 20mm x 20mm x 1.4mm and AK3671B is packaged in a 144-pin BGA with 10mm x 10mm x 1.25mm.

5.1 AK3671

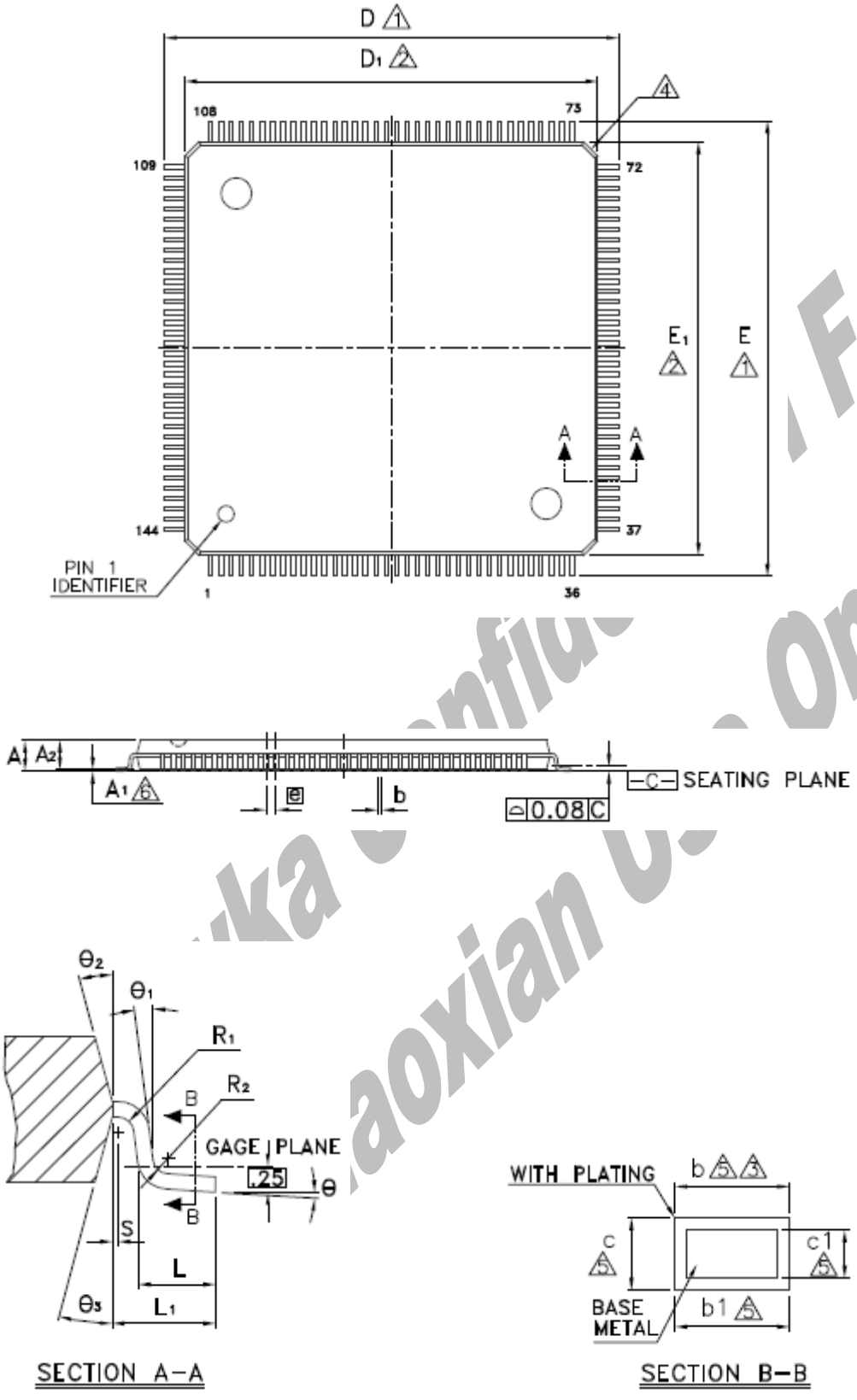
5.1.1 Pin Assignment

PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
1	GPIO[26]/ MPU_AD[12]	2	GPIO[27]/ MPU_AD[13]	3	GPIO[28]/ MPU_AD[14]
4	GPIO[29]/ MPU_AD[15]	5	GPIO[24]/ VIPCLK	6	GPIO[23]/ VISCLK
7	GPIO[22]/ VIPIXEL[0]	8	GPIO[21]/ VIPIXEL[1]	9	#NFC_CE[0]
10	VDDIO1	11	GPIO[30]/ #NFC_CE[1]	12	GPIO[31]/ MCK
13	TDO/ PCLK_OUT/ GPIO[14]	14	TDI/ I2S_DIO/ GPIO[13]	15	TMS/ I2S_LRCLK/ GPIO[12]
16	TCLK/ I2S_BCLK/ GPIO[11]	17	VSS1	18	GPIO[1]
19	GPIO[0]	20	VDD1	21	MDATA[15]
22	VSSIO1	23	MDATA[14]	24	MDATA[13]
25	MDATA[12]	26	MDATA[11]	27	MDATA[10]
28	#TRST	29	MDATA[9]	30	MDATA[8]
31	MDATA[7]	32	MDATA[6]	33	VSSIO2
34	MDATA[5]	35	MDATA[4]	36	MDATA[3]
37	MDATA[2]	38	MDATA[1]	39	VDDIO2
40	MDATA[0]	41	GPIO[20]/ VIPIXEL[2]	42	GPIO[19]/ VIPIXEL[3]

PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
43	GPIO[18]/ VIPIXEL[4]	44	GPIO[17]/ VIPIXEL[5]	45	MADDR[0]
46	MADDR[1]	47	MADDR[2]	48	SCAN_MODE
49	MADDR[3]	50	MADDR[4]	51	MADDR[5]
52	MADDR[6]	53	MADDR[7]	54	VSSIO3
55	MADDR[8]	56	MADDR[9]	57	MADDR[10]
58	MADDR[11]	59	MADDR[12]	60	GPIO[2]
61	GPIO[3]/ watch_dog/ VIPIXEL[6]	62	VDD2	63	#MBE[1]
64	#MBE[0]	65	MCAS	66	MRAS
67	VDDIO3	68	#MWR	69	MBA[0]
70	MBA[1]	71	#MCS	72	MCLK
73	MCKE	74	GPIO[16]/ VIPIXEL[7]	75	GPIO[15]
76	GPIO[10]/ UTD	77	GPIO[9]/ URD	78	GPIO[6]/ #SPI_CS
79	GPIO[5]/ VIVREF	80	USB boot/ GPIO[4]/ PWM	81	VSS2
82	VSSIO4	83	RTC_WU_WD	84	XTAL32KI
85	XTAL32KO	86	Vbat(RTC)	87	VSS (USB)
88	DP	89	DM	90	VDD33 (USB)
91	RREF	92	VDDA	93	NC
94	NC	95	HAVDD_DCAP	96	MIP_P
97	MIC_N	98	MIC_IN	99	Line_in
100	VCM	101	AVSS	102	AVDD/ LDO_V33A_O
103	R100K_TS	104	BANDGAP	105	HPL
106	HPR	107	SPVDD1	108	SPVSS1
109	AD0	110	AD1	111	SPKMINUS

PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
112	SPKPLUS	113	AD2	114	AD3
115	AIN	116	SPVSS2	117	DC_SW18
118	SPVDD2	119	VDDIO4/ LDO_V33D_O	120	AVDD18 (PLL)
121	DC_V18O/ VDD3	122	AVSS(PLL)/ VSS3	123	XTAL12MI
124	XTAL12MO	125	#RST	126	NFC_data[0]/ MPU_AD[0]/ MMC_data[0]
127	NFC_data[1]/ MPU_AD[1]/ MMC_data[1]	128	NFC_data[2]/ MPU_AD[2]/ MMC_data[2]	129	NFC_data[3]/ MPU_AD[3]/ MMC_data[3]
130	NFC_data[4]/ MPU_AD[4]/ MMC_data[4]	131	NFC_data[5]/ MPU_AD[5]/ MMC_data[5]	132	NFC_data[6]/ MPU_AD[6]/ MMC_data[6]
133	NFC_data[7]/ MPU_AD[7]/ MMC_data[7]	134	VSSIO5	135	NFC_CLE/ MPU_AD[8]/ SPI_MOSI
136	NFC_ALE/ MPU_AD[9]/ SPI_CLK	137	#NFC_WR/ MPU_AD[10]/ SPI_MISO	138	#NFC_RD/ MCMD
139	#MPU_WR	140	#MPU_RD	141	#MPU_CS
142	MPU_A0	143	GPIO[8]/ VIHREF	144	GPIO[25]/ MPU_AD[11]

5.1.2 Package Information



SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b_1		0.20 REF	
c	0.12	-	0.20
c_1		0.13 REF	
D	21.85	22.00	22.15
D_1	19.90	20.00	20.10
E	21.85	22.00	22.15
E_1	19.90	20.00	20.10
e		0.50 BSC	
L	0.45	0.60	0.75
L_1		1.00 REF	
R_1		0.15 REF	
R_2		0.15REF	
S		0.19 REF	
θ	0^0	3.5^0	7^0
θ_1		7^0 REF	
θ_2		12^0 REF	
θ_3		12^0 REF	

Notes:

1. To be determined at seating plane - c -.

2. Dimensions D_1 and E_1 do not include mold protrusion. D_1 and E_1 are maximum plastic body size dimensions including mold mismatch.

3. Dimensions b does not include dambar protrusion. Dambar can not be located on the lower radius or the foot.

4. Exact shape of each corner is optional.

5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the leap tip.

⑥ A_1 is defined as the distance from the seating plane to the lowest point of the package body.

7. Controlling dimension: millimeter.

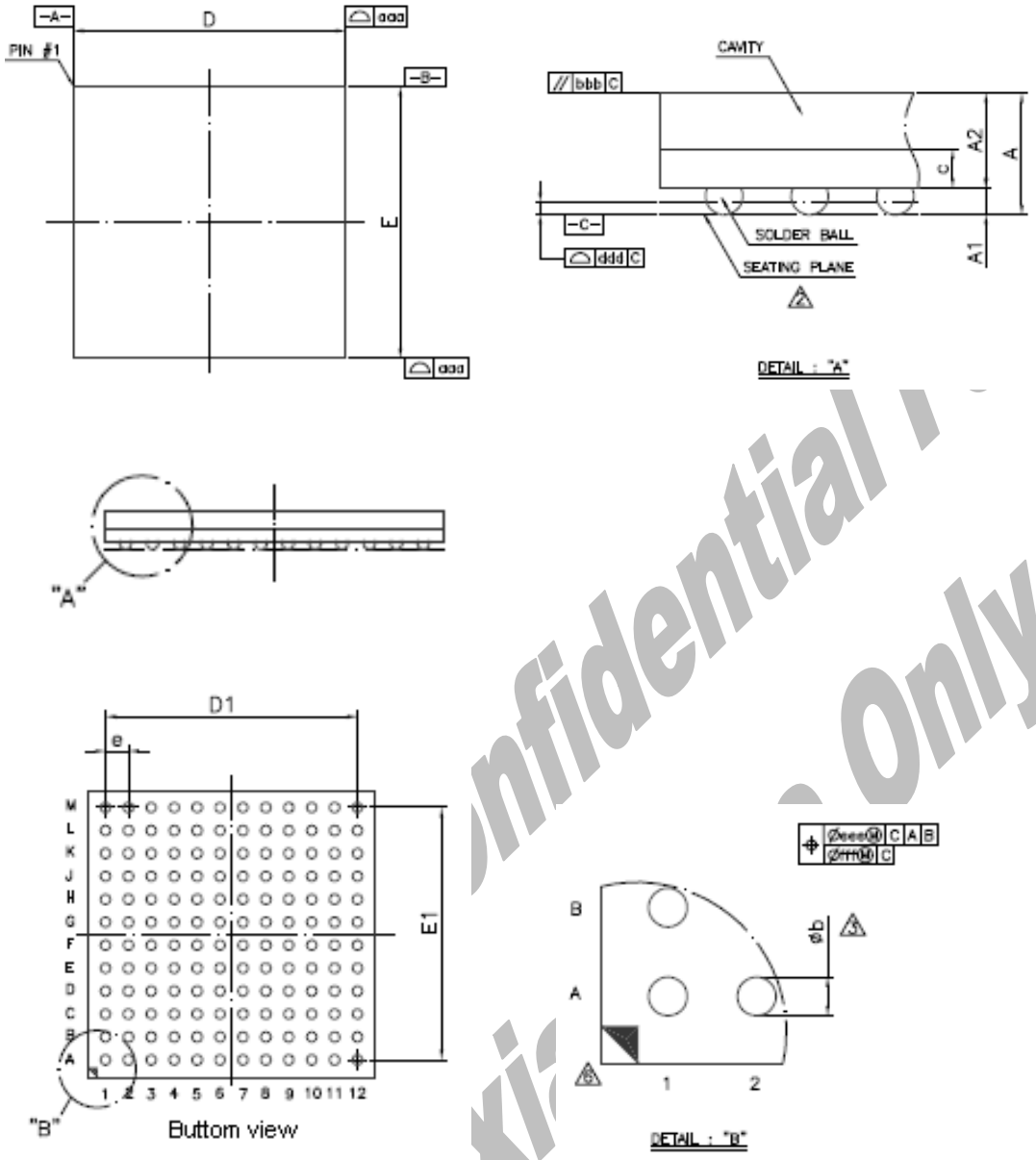
8. Reference document: JEDEC MS-026. BFB.

5.2 AK3671B

5.2.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12
A	SPVSS1	SPVDD1	HPL	BANDGAP	MIC_IN	RREF	XTAL32KI	GPIO[5]/ VIVREF	RTC_WU_WD	GPIO[10]/ UTD	GPIO[15]	MCKE
B	SPKPLUS	SPKMIMUS	HPR	R100K_TS	VCM	VDDA	DP	VSS (USB)	USB boot/ GPIO[4[/ PWM	GPIO[9]/ URD	GPIO[16]/ VIPIXEL[7]	MBA[0]
C	AD3	AD2	AD1	AVDD/ LDO_V33A_O	AVSS	NC	DM	VSSIO4	XTAL32KO	GPIO[6]/ #SPI_CS	MBA[1]	MCLK
D	SPVSS2	AIN	NFC_data[1]/ MPU_AD[1]/ MMC_data[1]	NFC_data[2]/ MPU_AD[2]/ MMC_data[2]	AD0	NC	VDD33 (USB)	Vbat (RTC)	VSS2	#MCS	#MWR	MADDR[12]
E	SPVDD2	DC_SW18	NFC_data[0]/ MPU_AD[0]/ MMC_data[0]	NFC_data[3]/ MPU_AD[3]/ MMC_data[3]	NFC_data[5]/ MPU_AD[5]/ MMC_data[5]	Line_in	HAVDD_DCAP	MCAS	MRAS	VDDIO3	MADDR[11]	MADDR[10]
F	VDDIO4/ LDO_V33D_O	AVDD18 (PLL)	AVSS (PLL)/ VSS3	DC_V18_O/ VDD3	NFC_data[6]/ MPU_AD[6]/ MMC_data[6]	MIC_N	MIC_P	#MBE[0]	#MBE[1]	VDD2	MADDR[9]	MADDR[8]
G	XTAL12MO	XTAL12MI	#RST	NFC_data[4]/ MPU_AD[4]/ MMC_data[4]	GPIO[1]	GPIO[18]/ VIPIXEL[4]	GPIO[17]/ VIPIXEL[5]	GPIO[2]	GPIO[3]/ watch_dog/ VIPIXEL[6]	MADDR[7]	MADDR[6]	VSSIO3
H	NFC_data[7]/ MPU_AD[7]/ MMC_data[7]	VSSIO5	GPIO[25]/ MPU_AD[11]	GPIO[26]/ MPU_AD[12]	GPIO[21]/ VIPIXEL[1]	GPIO[0]	GPIO[20]/ VIPIXEL[2]	GPIO[19]/ VIPIXEL[3]	SCAN_MODE	MADDR[5]	MADDR[3]	MADDR[4]
J	NFC_CLE/ MPU_AD_[8]/ SPI_MOSI	NFC_ALE/ MPU_AD[9]/ SPI_CLK	GPIO[8]/ VIHREF	GPIO[22]/ VIPIXEL[0]	TDO/ PCLK_OUT/ GPIO[14]	GPIO[30]/ #NFC_CE[1]	MDATA[14]	MDATA[13]	MDATA[6]	#TRST	MADDR[1]	MADDR[2]
K	#NFC_WR/ MPU_AD[10]/ SPI_MISO	#NFC_RD/ MCMD	MPU_A0	GPIO[23]/ VISCLK	GPIO[31]/ MCK	VSS1	VSSIO1	MDATA[10]	MDATA[7]	VDDIO2	MDATA[0]	MADDR[0]
L	#MPU_WR	#MPU_CS	GPIO[29]/ MPU_AD[15]	GPIO[24]/ VIPCLK	TDI/ I2S_DIO/ GPIO[13]	TMS/ I2S_LRCLK/ GPIO[12]	MDATA[15]	MDATA[11]	MDATA[8]	MDATA[4]	MDATA[2]	MDATA[1]
M	#MPU_RD	GPIO[27]/ MPU_AD[13]	GPIO[28]/ MPU_AD[14]	#NFC_CE[0]	VDDIO1	TCLK/ I2S_BCLK/ GPIO[11]	VDD1	MDATA[12]	MDATA[9]	VSSIO2	MDATA[5]	MDATA[3]

5.2.2 Package Information



SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	-	-	1.25
A1	0.20	0.25	0.30
A2	0.84	0.89	0.94
c	0.32	0.36	0.40
D	9.90	10.00	10.10

SYMBOL	MILIMETER		
	MIN	NOM	MAX
E	9.90	10.00	10.10
D_1	-	8.80	-
E_1	-	8.80	-
e	-	0.80	-
b	0.30	0.35	0.40
aaa		0.10	
bbb		0.10	
ddd		0.12	
eee		0.15	
fff		0.08	
MD/ME		12/12	

Notes:

1. Controlling dimension: millimeter

2. Primary datum c and seating plane are defined by the spherical crowns of the solder balls.

3. Dimensions b is measured at the maximum solder ball diameter, parallel to primary datum c.

4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.

5. Reference document: JEDEC MO-205.

6. The pattern of pin 1 fiducial is for reference only.

7. Special characteristic c class: bbb, ddd.